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Sustainability & Environmental Performance of Graphene-on-Silicon Hybrid Transistors: Green Fabrication, Low-Carbon Application and Circular E-Waste Mitigation

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Abstract. Conventional silicon-based semiconductor manufacturing relies on high-temperature thermal processes, toxic, corrosive chemical reagents, and significant wafer-cutting losses, generating enormous electronic waste and persistent carbon emissions throughout the entire industrial chain. Graphene-silicon hybrid field-effect transistors (GoSFETs) combine the mature processing compatibility of silicon wafers and ultra-high carrier mobility of single-layer graphene, achieving balanced electrical performance and environmental friendliness. Nevertheless, existing research mostly focuses on discrete device electrical characterization or on separate partial environmental tests, lacking a systematic full-life-cycle sustainability assessment that covers material synthesis, manufacturing, operation, and waste disposal. This paper firstly elaborates the heterostructure carrier transport mechanism of GoSFETs and introduces two classic interface wetting theories: the Wenzel model and the Cassie-Baxter model. Afterwards, the paper systematically sorts out low-carbon and low-toxic manufacturing technologies, including recycled carbon feedstock preparation and fully biodegradable biopolymer gate dielectric layers. The research further analyses the advantages of low-power operation in hybrid sensing devices and corresponding nano-carbon pollution prevention strategies. It constructs a complete closed-loop recycling workflow for end-of-life hybrid transistors. Supported by cradle-to-gate life cycle assessment (LCA) quantitative data, this study identifies core industrial bottlenecks that restrict large-scale mass production and proposes targeted optimization approaches. This research provides solid theoretical, process and industrial technical guidance for the future development of low-carbon, recyclable green graphene-silicon semiconductor devices.

Keywords: Graphene-on-Silicon FET, green electronics, life cycle assessment (LCA), circular economy, e-waste reduction

1. Introduction

Consumer electronics, wearable sensors, and IoT devices are widely used today, causing serious problems with electronic waste and high industrial carbon emissions. Traditional silicon-based MOS transistors require repeated high-temperature treatments and strong-acid polishing, while their oxide

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insulating layers cannot degrade naturally. This makes silicon devices highly energy-consuming and difficult to dispose of safely. Although pure graphene transistors perform well electrically at room temperature, they are limited by poor thermal stability, high production costs, and immature recycling technology. Graphene-on-silicon hybrid field-effect transistors (GoSFETs) combine the advantages of both silicon and graphene, offering a more environmentally friendly option for future electronic devices. Current research has explored the basic electrical properties and simple environmental impacts of GoSFETs [1-3]. However, few studies have analyzed how interfacial microstructure affects overall environmental performance throughout the device lifecycle, nor have they established a complete evaluation system for production, application, and waste recycling. This paper introduces the basic theories of interfacial wettability and sustainability, and then discusses green fabrication methods, low-power sensing applications, and closed-loop recycling solutions. The conclusion summarizes the industrial challenges and future research directions.

2. Theoretical basis of GoSFET and interface wettability

2.1. Structure and carrier transport mechanism of graphene-silicon hybrid transistor

GoSFETs are built on polished monocrystalline silicon as the base substrate, with single- or few-layer graphene serving as the conductive channel—the two materials bond through van der Waals forces, with no chemical reactions occurring at the interface. Early large-scale interface research found that dangling bonds, surface impurities, and uneven oxide layers on silicon surfaces disrupt carrier transport, thereby greatly weakening device performance [1]. To fix this issue, researchers developed low-temperature plasma growth techniques to improve silicon surface quality and thin the native oxide layer. This method reduces the heating energy needed for graphene growth by over 40% [2]. Further electrical tests on these hybrid transistors demonstrated that rough interface surfaces directly reduce the device on-off ratio, providing practical data to support structural optimization for improved environmental performance [3]. Overall, graphene channels help pure-silicon devices operate at lower voltages and consume less static power. Meanwhile, the silicon substrate provides graphene devices with solid mechanical support and tunable doping, improving thermal stability and reducing production costs.

2.2. Wenzel & Cassie-Baxter interface wetting theoretical model

Surface roughness at the interface plays a key role in two aspects: how uniform graphene films turn out during transfer and how likely nanocarbon particles are to leak out when devices are disposed of two well-known wetting models can quantify these effects. In the Wenzel model, liquid fills the tiny pits on the silicon surface, where roughness amplifies silicon's natural hydrophilic character and often causes graphene to stack unevenly. In contrast, once substrate roughness goes past a critical value, small air pockets get locked within surface features and create a mixed solid-liquid-gas contact state described by the Cassie-Baxter model, such rough, mixed-phase interfaces help graphene form even layers and physically separate graphene from the silicon substrate, meaning that when waste devices get crushed during recycling, those trapped-air gaps make graphene nanoparticles far less likely to break off and lower ecological risks from nanomaterial toxicity. The etch-and-print surface modification technique accurately controls silicon surface roughness to keep the system in a stable Cassie-Baxter regime, improving both the electrical performance and environmental safety of hybrid transistors [4].

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2.3. LCA evaluation system for electronic device sustainability

Life Cycle Assessment (LCA) acts as the standard quantitative tool to evaluate multi-dimensional environmental impacts of electronic devices across the whole lifespan. A complete cradle-to-gate LCA framework targeting all-carbon recyclable electronics has been established, taking carbon dioxide emissions, industrial water consumption, toxic organic reagent usage and solid waste output as core evaluation indicators [5]. Another LCA study quantifies the pollution load of traditional modified Hummer's graphene synthesis, proving that waste acid and heavy metal residues from graphite oxidation constitute the primary environmental burden of graphene raw material preparation [6]. Combining the two existing LCA systems, this paper constructs a targeted evaluation framework exclusive to GoSFET, which separates the environmental contribution of silicon pretreatment, graphene transfer, dielectric deposition and inkjet printing links, providing measurable quantitative standards for green process upgrading.

2.4. Performance comparison of silicon-only and pure graphene devices

Monocrystalline-silicon transistors benefit from well-established industrial manufacturing workflows, yet wafer cutting produces huge volumes of silicon powder waste. They also use non-degradable inorganic dielectrics that cannot break down in the natural environment. Pure-graphene transistors deliver extremely high carrier mobility, but they are limited by weak thermal stability under prolonged operation, high costs to produce large-area films, and recycling methods that are still not practical. GoSFET offers a sensible balance between device performance and environmental impact. With graphene-seeding pre-treatment, silicon wafer surface texture can be adjusted, and cutting-related waste can drop by 60% relative to conventional silicon fabrication [7]. Using biopolymer gate dielectrics instead of inorganic oxides or plastic insulators allows devices to degrade naturally at the end of their life, avoiding long-lasting solid-waste pollution from electronics [8].

3. Low-carbon green fabrication process of GoSFET

3.1. Low-waste silicon substrate pretreatment technology

Standard silicon wafer fabrication uses mechanical polishing and high-temperature strong-acid etching, which generates large amounts of silicon-powder solid waste and highly acidic wastewater. Graphene-seeding pretreatment deposits small graphene nuclei on silicon surfaces, changing their micro-scale surface features. This reduces material loss by 60%, while forming stable Cassie-Baxter wetting interfaces [7]. Used together with low-temperature plasma cleaning, this pretreatment avoids high-temperature corrosive polishing chemicals, so toxic waste in factory wastewater drops significantly [2]. The etch-print surface modification approach can adjust interface roughness near the Cassie-Baxter critical condition. It improves the success rate of graphene transfer by over 30%, and wastes less material during mass production [4].

3.2. Environment-friendly graphene preparation and transfer route

The commonly modified Hummers' method for producing graphene uses large quantities of concentrated sulfuric acid and potassium permanganate. It produces wastewater containing heavy-metal manganese ions and has a very large carbon footprint, as supported by LCA quantitative data [6]. Instead, upcycling methods can produce high-quality graphene from waste

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plastic polymer substrates. This turns industrial solid waste into functional electronic materials and makes carbon resources reusable [9]. Water-based graphene conductive ink eliminates poisonous organic solvents such as NMP. It allows transistors to be printed at room temperature in roll-to-roll processes, so no polluting volatile organic compounds are released while patterning graphene [10]. Low-carbon inkjet printing improves ink flow and compatibility with different substrates. It removes energy-hungry high-temperature annealing steps, lowering total carbon output during production by almost 35% [11].

3.3. Biodegradable biopolymer gate dielectric material

Inorganic silicon oxide and petroleum-based plastic dielectric layers are the major sources of non-decomposable electronic waste after device retirement. Biopolymer-gated graphene transistors use natural biomass macromolecules, including chitosan and sodium alginate, as gate insulating layers that fully degrade within 3–6 months in soil and freshwater environments, leaving no residual toxic ions [8]. This biomass dielectric material matches the low-temperature printing manufacturing flow of biodegradable graphene pressure-sensitive FETs, laying the core material foundation for fully transient zero-residue electronic sensing equipment [12]. Unlike traditional rigid inorganic insulators, biopolymer dielectrics also have flexible mechanical properties, making them suitable for wearable flexible hybrid transistor applications.

3.4. Room-temperature inkjet printing mass production scheme

Water-based graphene ink forms a low-energy room-temperature printing manufacturing route for low-power GoSFETs, avoiding high-vacuum deposition and photolithography processes with huge energy consumption [10]. Optimized low-carbon inkjet printing technology adjusts ink viscosity and substrate surface affinity, realizing batch preparation of hybrid transistors without any high-temperature thermal treatment [11]. Laser ablation additive manufacturing serves as an auxiliary solvent-free molding process for special-shaped fully biodegradable carbon transistors, eliminating organic solvent pollution during device shaping and expanding the application range of green printing technology [13]. The integrated room-temperature printing system cuts toxic chemical usage and production power consumption by over half compared with traditional semiconductor manufacturing lines.

4. Sustainable application and environmental risk control

4.1. Low-power energy-saving application scenarios of hybrid transistors

Graphene conductive channels with ultra-high carrier mobility reduce device operating voltage and static power consumption, forming multiple low-power long-term monitoring application scenarios. Molecular-modified graphene hybrid transistors act as low-energy operando optoelectronic testing platforms, suitable for unattended environmental monitoring sensors with ultra-low battery power supply demand [14]. Inkjet-printed flexible GoSFETs are widely applied to wearable health sensing equipment, extending battery service life and lowering indirect carbon emissions caused by frequent power supply replacement throughout the whole service cycle of terminal electronic products.

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4.2. Biodegradable transient sensing electronic devices

Biodegradable graphene pressure-sensitive FETs can be completely decomposed in natural environments after finishing short-cycle monitoring tasks, removing the recycling burden of disposable electronic devices and avoiding massive, short-life e-waste accumulation [12]. Laser ablation additive manufacturing can produce fully degradable carbon transistors matched with biopolymer dielectrics, applicable to temporary medical implant sensors and agricultural soil monitoring equipment with zero-pollution abandonment requirements [13]. Such transient electronic products fundamentally solve the problem of difficult recovery of disposable miniature sensors.

4.3. Nano-carbon toxicity control of waste electronic devices

Once GoSFET devices reach the end of their service life, a key hidden environmental risk appears graphene nanoparticles can break free when the hardware is mechanically crushed. The rough Cassie-Baxter interface created by etch-print pretreatment forms a physical barrier between the graphene channel and the silicon substrate. This barrier helps limit nanoparticle detachment during crushing and waste-sorting processes [4]. Toxicology work on graphene-silicon hybrid e-waste shows that simply grinding up old hardware releases nano-carbon particles, which may build up in natural ecosystems over time. Layer-separation recycling offers a practical way to capture these loose carbon particles and reduce associated toxic risks [15]. Implementing a full closed-loop recycling workflow is therefore critical, as it largely stops large amounts of these nanoparticles from spreading into the environment.

4.4. Practical industrial application cases

Several pilot tests have been carried out for real-world use cases, including flexible wearable biosensors, disposable environmental monitoring devices and low-power optoelectronic detector chips. Low-carbon inkjet printing has been used to make small test runs of hybrid transistors on lab-based pilot lines [11]. Graphene-seeding pretreatment for silicon wafers has also been trialed on wafer pilot equipment, with real-world results showing less material waste and lower substrate-related costs [7]. Graphene produced by upcycling waste polymer materials can now be supplied consistently at laboratory scale, providing low-cost, eco-friendly carbon feedstock for future device fabrication [9]. These pilot results demonstrate that such green manufacturing techniques can work in practical settings. Even so, two major bottlenecks remain before full-scale roll-out: overall production costs are still relatively high, and interface performance tends to drift over long-term device operation.

5. Circular economy scheme for waste GoSFET

5.1. Closed-loop recycling technology for waste GoSFET

By leveraging the physical isolation effect of Cassie-Baxter composite interfaces, layered separation recycling enables non-destructive separation of graphene conductive channels from silicon substrates without overall pulverization. Separated silicon wafers can return to the substrate pretreatment production line after simple surface cleaning and oxidation removal. At the same time, recycled graphene films can be reprocessed into water-based conductive ink for new transistor channel preparation [4, 9]. This layered recovery mode avoids the nano-carbon particle leakage risks identified in hybrid electronic waste toxicology research [15]. It greatly reduces the demand for

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virgin graphite and monocrystalline silicon raw material extraction, realizing closed-loop circular utilization of core functional materials.

5.2. Optimization improvement strategies for green hybrid transistors

Targeted optimization strategies are proposed for existing manufacturing and performance defects. To improve heterojunction thermal stability, low-temperature plasma growth parameters can be fine-tuned to reduce interface oxide-layer defects and limit carrier thermal scattering [2]. To reduce manufacturing costs, the production scale of waste-polymer-upcycled graphene should be expanded to lower the unit price of carbon functional materials [9], and graphene seeding pretreatment should be widely promoted to cut silicon raw material consumption and wafer waste [7]. For long-term interface performance stability, etch-print process parameters need precise adjustment to lock a stable Cassie-Baxter wetting state and extend device service life and recycling cycles [4]. Large-scale full-chain LCA industrial trials should be carried out to quantitatively evaluate the economic and environmental comprehensive benefits of all optimized processes [5, 6].

6. Conclusion

This research examines the sustainability of graphene-silicon hybrid transistors across their entire life cycle, from design and manufacturing to daily operation and final recycling. The Cassie-Baxter rough interface constructed in this study not only makes graphene films more uniform but also physically locks graphene in place, preventing nanoparticle shedding and pollution when devices are discarded. By recycling graphene from waste plastics, adopting biodegradable polymer dielectrics, and printing devices at room temperature, our manufacturing process greatly reduces material waste, harmful chemical use, and overall carbon emissions. These low-power and degradable GoSFET devices also consume less energy during operation and leave no permanent electronic waste after use.

Although layered recovery techniques can recycle and reuse both silicon and graphene, large-scale industrial production still faces clear limitations. The graphene-silicon junction struggles with long-term thermal stability, eco-friendly recycled materials remain expensive, and gradual changes in surface wetting conditions shorten device lifespan. LCA data show that recycled graphene and biodegradable materials are the main cost barriers to industrial adoption [5, 6], and pilot production also shows that green pretreatment and low-carbon printing inevitably increase processing costs [7, 11].

Future work can proceed in three main directions: develop fully degradable, biomass-based transistor structures based on current biopolymer dielectric technology [8], conduct complete industrial LCA tests on official production lines to obtain real environmental impact data [5], and improve low-cost mass production methods for waste-recycled graphene to lower material costs [9]. Optimizing low-temperature plasma growth and etch-print interface regulation will improve thermal stability and reduce long-term interface performance decay [2, 4]. Scaling up graphene seeding pretreatment and low-carbon printing technologies will further cut silicon waste and production carbon emissions [7, 11]. Overall, this multi-stage study provides practical theoretical and technical guidance for designing greener, low-carbon, and recyclable next-generation semiconductor devices.

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