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A Review of Novel Chip Technologies amid the Slowdown of Moore's Law

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Abstract. As integrated circuit scaling approaches atomic limits, traditional process nodes face severe quantum tunneling and thermal constraints, which decelerates the progression of Moore's law. To satisfy high-performance computing demands for greater power efficiency and integration density, Chiplet technology—based on "partition-first, integration-later" and heterogeneous integration—has emerged to extend Moore's Law by improving yield, reducing design complexity, and enabling module reuse. Advanced packaging provides the physical foundation for Chiplets across three dimensions: 2D planar interconnection offers low-cost, mature manufacturing and uses high-density bridges for basic chiplet-to-chiplet electrical connections. 2.5D passive silicon interposers utilize ultra-fine routing and through-silicon vias to bypass conventional layout routing limits, which enhances signal integrity and reduces RC delay. 3D vertical stacking employs advanced hybrid bonding to eliminate solder bumps, which achieves molecular-level integration that minimizes compute-to-memory physical distance while maximizing bandwidth and power efficiency. Finally, applying heterogeneous automotive SoC to intelligent driving systems is critical for integrating multimodal environmental sensing data from HD cameras, LiDAR, and radar. The transition from monolithic ICs to 3D heterogeneous integration represents a key pathway to overcoming physical limitations and realizing highly integrated computing for smart automotive control. Addressing the physical, manufacturing, and latency challenges associated with this integration will provide vital guidelines for future chip design.

Keywords: Moore's Law, Chiplet, Advanced Packaging, Automotive Heterogeneous Chips, Intelligent Driving

1. Introduction

Since the late 20th century, global IT growth has been driven by Moore's Law. Continuous transistor scaling successfully integrated more functions onto single chips [1]. However, as electronics demand extreme integration and miniaturization, chip complexity rises exponentially while process node scaling approaches physical limits. Currently, scaling faces two core barriers [2]: Quantum Tunneling: When transistors shrink to atomic scales, insulation layers leak electrons, causing current leakage, heating, and logic errors. Thermal and Power Walls: Ultra-dense transistors generate extreme heat. Inadequate dissipation causes permanent damage or downclocking, limiting clock

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frequencies. As monolithic manufacturing costs soar and yields plunge, the industry requires transformation. To meet demand for high bandwidth, low latency, and high computing power in CPUs and GPUs, heterogeneous integration—particularly Chiplet technology—has emerged to bypass Moore's Law bottlenecks. The core of Chiplets is "disaggregation before integration." Conventional SoCs break down complex blocks into smaller Chiplets, each with a dedicated function [3]. Advanced packaging and internal buses then reintegrate Chiplets from different nodes or functions into modular, customized designs [3]. This cuts die size, boosts yield, and lowers cost, while also offering high flexibility and reusability—all of which accelerate design cycles. Throughout this process, advanced packaging plays a key role in addressing power, thermal, and cost challenges [4]. This technology is reshaping high-computing scenarios, notably intelligent driving. Modern autonomous driving demands stringent computing power and efficiency [5]. For perception, diverse sensors require real-time data fusion. To eliminate latency from early modular designs, modern controllers now use heterogeneous SoC architectures. These integrate AI accelerators for parallel feature extraction, multi-core CPUs for decision-making and path planning, and GPUs for image preprocessing—all while delivering high performance within the tight space of vehicles [5].

2. Analyzing the physical limits facing Moore's Law

2.1. Physical limit 1: quantum tunneling effect

Early integrated circuit designs advanced under Moore's Law, with engineers scaling feature dimensions down to pack more transistors onto individual silicon dies [2]. However, at the atomic scale, classical physics gives way to quantum effects. Among these, the quantum tunneling effect poses a physical bottleneck for further scaling. When insulation layers become extremely thin, electrons can tunnel through the insulator barrier, creating unpredictable leakage current. Such electron leakage raises overall chip power draw, amplifies thermal buildup, and introduces random hardware calculation errors.

2.2. Physical limit 2: thermal and power walls

Future product trends lean toward highly integrated functions and extreme miniaturization [2], exponentially increasing chip complexity [1]. Consequently, Moore's Law development faces growing difficulties as feature sizes approach physical limits, while costs skyrocket because of the quantum tunneling effect and the thermal and power walls [2]. These walls stem from excessive transistor density per unit area, where rapid switching releases massive power that converts into thermal energy, escalating heat density. In space-constrained environments like automotive or high-performance computing systems, failing to dissipate this heat in time causes physical damage. To protect the hardware, systems trigger automatic downclocking mechanisms. This keeps clock frequencies from rising indefinitely, which ultimately limits single-core performance growth and makes reliance on advancing process nodes insufficient for evolving demands.

3. Theoretical architecture and core advantages of Chiplet technology

3.1. The background and conceptual definition of the rise of Chiplet technology

As process scaling approaches atomic limits, the monolithic model faces bottlenecks like quantum tunneling and power walls, slowing Moore's Law. Concurrently, big data and AI pose severe

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performance challenges for CPUs and GPUs, and demand higher bandwidth, greater computing power, and lower power consumption. Because scaling alone no longer suffices, heterogeneous integrated chip technology has emerged [4]. Chiplet technology is a modular, customized approach that uses buses and advanced packaging to integrate dies of different processes or functions. This approach effectively breaks a traditional SoC into functional Chiplet combinations [3]. Its core philosophy is "disaggregation before integration"—first disassembling complex functional blocks within a monolithic chip, and then using advanced packaging to reintegrate these interconnectable, modular dies into a cohesive network. In this integration phase, critical functional components are consolidated, which calls for a careful balance of power consumption, thermal dissipation, and cost constraints [4].

3.2. Core advantages and value of Chiplet technology

Disaggregating a chip into standardized modules reduces defects and cuts costs, while flexibility and reusability speed up iteration cycles. It enables multi-core integration for high-performance processors while reducing design complexity. This approach delivers four core advantages: Yield Advantage: When monolithic chip areas approach reticle limits, yields drop sharply. Chiplet technology adopts a "divide and conquer" method, breaking a large chip into smaller functional dies to bypass the yield penalties of extreme die sizes. Cost Advantage: Heterogeneous integration matches each module with its optimal process node. Computing cores utilize expensive advanced nodes, while process-insensitive components like I/O and memory leverage lower-cost mature nodes. Advanced packaging then stitches them to optimize system costs. Reusability: Chiplets transform complex functions into modular hardware building blocks. Rearranging identical blocks across different product lines maximizes the amortization of one-time photomask R&D costs and eliminates redesigning from scratch, which also accelerates market iteration. Computing Scalability: Utilizing ultra-high-bandwidth and low-latency packaging interfaces, Chiplet technology seamlessly connects multiple large dies in 2.5D or 3D configurations. At the OS level, these separate dies operate as a single unified monolithic chip, which shatters single-wafer manufacturing ceilings and thus enables virtually limitless scaling of computing power and transistor density.

4. Classification and architectural evolution of advanced Chiplet packaging technologies

4.1. Overview of Chiplet interconnect mediums and packaging dimensions

Chiplet packaging stacks dies using Through-Silicon Vias, stitches them via silicon bridges, or connects them using active or passive interposers across 2D, 2.5D, and 3D dimensions. 2D Packaging: Arranges chips side-by-side on a flat plane without silicon interposers, relying on traditional organic substrates or redistribution layers. However, it suffers from bandwidth, power, latency, and interference bottlenecks. 2.5D Packaging: Stacks chips side-by-side but inserts a silicon interposer between the chips and the substrate. With micro-bumps, ultra-short routing, and vertical TSVs, it overcomes 2D limitations in bandwidth, power, and electromagnetic interference. 3D Packaging: Vertically stacks chips in 3D space rather than horizontally, aligning them in face-to-face or face-to-back configurations.

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4.2. 2D packaging planar direct interconnect architecture

2D packaging with direct interconnects places multiple dies or components side-by-side on a substrate's x-y plane, using wire bonding or flip-chip techniques for electrical connections and without an extra interposer. A representative example is AMD's interconnect method for joining multiple Chiplets, driven by two core structures: a scalable data fabric and a scalable control structure [6]. The data fabric transfers data between cores and memory across different Chiplets, while the control structure manages system signals like power and clock synchronization to maintain precise alignment at low system levels [6]. However, growing computing demands expose severe bottlenecks in 2D packaging: Bandwidth Wall: Organic substrate wiring density lags behind monolithic chips by orders of magnitude. As cores multiply, perimeter pin saturation prevents substrates from providing enough parallel channels, bottlenecking high-bandwidth memory and intensive data exchanges. Power Wall: Long organic substrate wires create parasitic capacitance and resistance, resulting in RC delay. To prevent signal attenuation, Chiplets need large, high-output I/O drivers, which drive up energy consumption per bit and push the total power budget to its limit. Latency and Interference: Long-distance, parallel routing triggers electromagnetic interference and signal reflection. This distorts receiver waveforms, hindering accurate signal distinction.

4.3. 2.5D packaging horizontal integration based on passive interposers

In 2.5D packaging, chips are horizontally stacked and interconnected on a silicon interposer that contains Through-Silicon Vias and high-density metal lines, which avoids a 3D vertical stack [7]. When this platform contains no active circuitry and features only TSVs and metal routing to connect chips and route signals, it is referred to as a passive interposer [6]. Table 1 below compares the internal structures, power consumption, signal transmission, and other characteristics of 2.5D active and passive interposers.

Table 1. Structural comparison between 2.5D active and passive interposers

Structure and Technology	2.5D Passive Interposer	2.5D Active Interposer
Manufacturing Process Requirements	Only back-end processes required	Both front-end and back-end processes required
Internal Structure	High-density metal routing, TSVs	Logic gates, TSVs
Signal transmission method	Wire conduction	Active routing scheduling, signal amplification
Power consumption	Zero power consumption	Has dynamic power consumption
Transistor	None, pure passive silicon substrate	Yes, integrates a large number of logic circuits

Passive interposer technology presents distinct trade-offs in 2.5D system integration: Advantages: Excellent Heat Dissipation: Lacking active devices like transistors, passive interposers consume zero switching power and generate no operating heat. This allows upper chips to dissipate heat directly through the top heatsink. High Manufacturing Yield: Requiring only back-end fabrication without complex, scaled front-end transistor manufacturing, production difficulty is significantly reduced. Clean EMI Environment: The absence of active switching circuits eliminates high-frequency transistor switching noise, preserving signal integrity for interconnects. Disadvantages: Lack of Signal Amplification: Offering only physical wire connections, horizontal scaling increases distances between distant chiplets, accumulating parasitic resistance and capacitance. Without active

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repeaters or buffers, signals attenuate over long distances. High-Frequency Instability: During high-performance computing, sudden full-load operations trigger current fluctuations. Because the passive interposer lacks active voltage regulators right beneath the chiplets for local voltage compensation, power must travel vertically from the substrate through long TSVs. According to Ohm's Law, the wire resistance causes a transient voltage drop that can trigger computing errors at high frequencies. Large Horizontal Footprint: Because chiplets are laid out horizontally on a two-dimensional plane, this configuration still consumes a massive amount of horizontal package area despite overcoming traditional 2D bandwidth limitations.

4.4. 3D vertical stacking and hybrid bonding technology

3D packaging builds upon 2.5D technology to further compress bump density and break through planar integration limits [4]. It directly stacks chips and chiplets vertically for three-dimensional integration [8], utilizing space more efficiently [9]. Internally, it uses through-silicon vias for vertical interconnection, along with passive or active interposers or microbumps, to achieve high-density vertical interconnection. This technology has become a vital path for extending Moore's Law, bringing three key advantages: Ultra-thin Form Factor: Advanced hybrid bonding utilizes molecular-level direct Cu-Cu and silicon dioxide dielectric bonding. This eliminates traditional solder bumps and narrows interconnect gaps, reducing overall stack thickness [4]. Reduced Latency and Power Consumption: Vertical stacking dramatically shortens the physical distance between compute and memory units, minimizing parasitic effects. Lowering channel capacitance and inductance effectively solves RC delays and I/O transmission power consumption caused by long routing. Enhanced System Performance: Shortened paths and scaled pin pitches accelerate data speeds. Free from 2D routing limitations, parallel transmission across channels significantly boosts system performance and bandwidth. Based on wafer-to-wafer and chip-to-wafer hybrid bonding, 3D integration falls into three categories [10]:

3D System-in-Package: Package-level integration including package-on-package and 2.5D multi-chip modules using interposers. 3D Integrated Circuits: Chip-level integration featuring vertical stacking interconnected via microbumps or TSVs. 3D System-on-Chip: High-density wafer-level integration utilizing wafer-to-wafer direct bonding from the circuit design phase.

5. Automotive heterogeneous chips and intelligent driving multi-sensor fusion

5.1. Intelligent driving system architecture and challenges

Intelligent driving encompasses all automotive automation, and its driving systems comprise perception, prediction, control, and planning modules [5]. Early modular designs used independent modules that relied on 3D physical coordinates for static data alignment. Although boundaries were clear, excessive software layers and serial processing caused information latency and degraded real-time response. The goal of intelligent driving is safe, autonomous operation in complex environments. This relies on intelligent vehicle technology, which encompasses software functional systems and hardware support like sensors, controllers, actuators, and automotive computing chips. These chips provide critical computing power; integrating multi-core CPUs, GPUs, and sensor interfaces onto them reduces both physical footprint and power consumption.

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5.2. Comparison of characteristics of diverse environmental perception sensors

The automotive environmental perception system relies on HD cameras, millimeter-wave radars, and LiDARs. However, these sensors differ significantly in detection principles, environmental adaptability, and inherent limitations. Table 2 below details a horizontal comparison of these three dimensions.

Table 2. Comprehensive comparison table of performance parameters for mainstream automotive perception sensors

Comparison Dimension	HD Camera	Millimeter-Wave Radar	LiDAR
Core Detection Principle	Capture optical signals	Measure relative distance	Generate 3D point clouds
Environmental Adaptability	Weakest adaptability	Strongest adaptability	Moderate adaptability
Target Recognition Capability	Accurately identify lanes	Unaffected by rain	Unaffected by light
Detection range	Lack of distance sensing	Detect deceleration of vehicle ahead	Centimeter-scale distance sensing
Advantages	Lower cost	Stronger penetration	Higher detection accuracy
Typical use cases	Traffic Sign Detection	Brake system detection	Night obstacle avoidance
Disadvantages	Reduced detection accuracy in tunnel	Lower resolution	Reduced detection in rain

Vehicle sensors are classified into environmental perception sensors—the "eyes" of intelligent driving that detect obstacles, pedestrians, and lanes—and vehicle state sensors. Environmental perception hardware includes: HD Cameras: Capture light via CMOS sensors and output 2D images, and precisely recognize lane markings and traffic signs. However, they lack distance-sensing capabilities and suffer from degraded recognition under sudden light changes. LiDAR: Emits laser pulses to construct 3D point clouds via photon time-of-flight and achieves centimeter-level distance precision. As an active light source, it works at night but is costly, complex to manufacture, and prone to signal scattering in heavy rain or smoke. Millimeter-Wave Radars: Millimeter-Wave Radars: Emit millimeter-band electromagnetic waves and use the Doppler effect to measure object distance and speed. As an all-weather sensor, it excels at detecting vehicle deceleration in rain or darkness [5]; however, its low resolution can cause it to miss pedestrians or non-metallic objects due to their small radar cross-sections.

5.3. Core architecture and functional allocation of automotive heterogeneous SoC

The controller serves as the vehicle's brain, adopting a heterogeneous chipset architecture where different computing cores work collaboratively. This architecture is realized through high-performance automotive-grade SoCs and consists of three core components: AI Deep Learning Accelerator: handles massive parallel computations for real-time feature extraction and multi-sensor data fusion. Multi-core CPU: runs prediction algorithms, makes behavioral decisions, plans paths, and hosts safety-critical automotive operating systems—all within complex serial logical operations. GPU: Assists in high-bandwidth visual computing tasks, such as image preprocessing and spatial geometric transformations. In operation, these components work in synergy across three sequential stages: Preprocessing: Raw data from cameras and LiDAR enters a unified memory, where the GPU performs format conversion and pixel alignment, turning raw data into standardized feature matrices. Perception and Fusion: The AI accelerator processes these matrices through deep neural

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networks for object recognition and fuses visual and point cloud features to construct a structured dynamic environmental map. Decision and Planning: The CPU receives this map, runs prediction algorithms to assess surrounding vehicles, determines actions, calculates the optimal path, and dispatches validated control commands to the chassis.

6. Conclusion

As scaling approaches physical limits and slows Moore's Law, traditional monolithic nodes face quantum tunneling and thermal walls, which drive up costs and reduce yield. To satisfy high-performance computing demands, the semiconductor industry is shifting toward "More-than-Moore" via Chiplet technology. With heterogeneous integration, Chiplets disassemble monolithic designs into modular, reusable dies, which reduces complexity and boosts yield. Advanced packaging provides the physical foundation for Chiplets. This technology has evolved from 2D planar interconnections, to 2.5D integration utilizing passive silicon interposers and through-silicon vias, and ultimately to 3D vertical stacking using hybrid bonding. This dimensional evolution shortens compute-to-memory physical distance and eliminates parasitic effects, which helps sustain Moore's Law. Finally, when applied to intelligent driving, these technologies allow heterogeneous automotive SoCs to replace single-function systems and process diverse sensor data from HD cameras and LiDAR. Future trends focus on overcoming computing limits through microfluidic cooling and high-thermal-conductivity materials. However, one research limitation is that we lack a theoretical model to address internal stress fatigue and thermomechanical failures in 2.5D/3D packaging subjected to extreme automotive-grade thermal cycling and vibration.

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