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Research Progress and Prospects of Integrated Circuit Reliability Technology

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Abstract. With the continuous scaling of semiconductor processes and the wide application of 3D heterogeneous integration technology, integrated circuit reliability is facing unprecedented challenges. This paper systematically reviews the latest domestic and international research results in the field of integrated circuit reliability from 2022 to 2026, compares and analyzes the characteristic advantages of foreign basic mechanism research and domestic engineering application innovation, elaborates core theoretical methods such as physics-based failure modeling and multi-physics field coupling simulation, analyzes the practical value of technology combined with typical scenarios such as aerospace and automotive electronics, dissects current technical bottlenecks like multi-scale coupled failure, and prospects future development directions such as intelligent active health management. This paper can provide reference for theoretical research and engineering practice in the field of integrated circuit reliability.

Keywords: Integrated circuit reliability, failure mechanism, multi-physics field coupling, advanced packaging, intelligent prediction, lifetime evaluation

1. Introduction

1.1. Research background and strategic significance

Integrated circuit reliability is the core guarantee for the long-term stable operation of modern electronic systems, and its importance has become increasingly prominent with the continuous scaling of semiconductor processes and the exponential growth of system complexity. From consumer electronics to aerospace, from artificial intelligence accelerators to power transmission networks, the robustness of almost all critical infrastructures and cutting-edge applications directly depends on the ability of underlying integrated circuits to resist various stresses and failure mechanisms within their expected lifetime [1]. Reliability is not only related to product safety and service life, but also a key support for measuring the maturity of semiconductor technology and promoting its development to more advanced nodes.

While process scaling brings performance improvement and power consumption reduction, it also introduces more severe reliability challenges such as time-dependent dielectric breakdown of gate oxide, hot carrier injection, electromigration and interconnect delay. These problems are particularly acute in fields with strict requirements on bandwidth and energy efficiency, such as

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high-performance computing and high-speed communication. The wide application of advanced packaging and integration technologies, such as 2.5D/3D packaging based on through-silicon vias (TSV) and Chiplet heterogeneous integration, has brought new reliability risk points while improving system performance and integration density [2]. The filling uniformity of TSVs themselves, the mechanical integrity of microbump interconnections, and the thermomechanical stress caused by multi-chip multi-physics domain coupling have become key factors affecting system-level reliability [3]. Similarly, in monolithic three-dimensional integrated circuits, high-density interlayer vias (ILV) face various potential failure modes such as open circuits and short circuits, requiring special test methods to ensure the interconnection quality after bonding [4].

At the same time, third-generation wide-bandgap semiconductor devices such as gallium nitride high electron mobility transistors (HEMT) are gradually moving from research and development to large-scale application, and their unique material properties and physical mechanisms make traditional reliability evaluation models and methods face update requirements. Studies have shown that under reverse conduction operation mode, p-GaN HEMT will undergo degradation at different time scales at the AlGaN barrier layer and metal-semiconductor junction at the gate edge, leading to threshold voltage drift and eventual failure [5]. This indicates that research on the reliability mechanism of new materials must be carried out ahead of productization to prevent potential field failures. In addition, as a potential source of electromagnetic interference, the radiation emission level of integrated circuits is directly related to the electromagnetic compatibility of the entire electronic system, thereby affecting the reliable operation of co-located equipment. Standard radiation emission test methods, such as TEM or GTEM cell method and surface scanning method, provide a unified benchmark for quantitatively evaluating the electromagnetic interference potential of chips [6, 7]. Therefore, integrated circuit reliability research is a three-dimensional technical system that runs through materials, devices, circuits, packaging and system applications, and its development has indispensable strategic significance for breaking through technical bottlenecks and ensuring the safety of the industrial chain.

1.2. Research scope and framework of this paper

The research scope of this paper focuses on multi-level failure mechanisms and guarantee technologies from underlying devices to top-level systems. At the device level, it involves the inherent reliability and degradation behavior of silicon-based and emerging materials such as SiGe, GaN, and SiC. For example, while SiGe channel CMOS devices improve NBTI characteristics, they also face a series of challenges such as intensified PBTI, decreased gate oxide breakdown voltage, and severe self-heating effects. Research at the circuit level extends to reliability modeling and noise suppression of specific functional modules, including modeling and optimization of power supply noise caused by package parasitic parameters in on-chip low-dropout regulators, as well as accurate reliability prediction for power converters used in LED driving. System-level reliability assurance needs to cope with more complex interactions and harsh environments, including studying the functional robustness of integrated circuits under extreme temperature cycling and radiation conditions, such as developing radiation-hardened designs for the dual-node upset problem of aerospace SRAMs, and exploring the long-term threat of aging stress to the electromagnetic immunity performance of integrated circuits.

The core goal of this paper is to systematically sort out the complete methodology from failure physics models to system-level robustness evaluation through cross-level collaborative analysis and design, so as to address the new reliability bottlenecks brought by process scaling, 3D integration and complex application scenarios. The structure of the full text is arranged as follows: Chapter 2

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compares and analyzes the latest research progress and characteristic breakthroughs in the field of integrated circuit reliability at home and abroad; Chapter 3 elaborates on the core theoretical methods of reliability modeling and evaluation; Chapter 4 analyzes the practical value of technology combined with typical application scenarios such as aerospace and automotive electronics; Chapter 5 dissects the current technical challenges and bottlenecks; Chapter 6 prospects future development trends and cutting-edge research directions; finally, Chapter 7 summarizes the full text. This paper focuses on sorting out the latest research results from 2022 to 2026, striving to fully reflect the technical status and development dynamics of this field, and provide reference for theoretical deepening and technological innovation in related fields.

2. Domestic and foreign research status and comparative analysis

2.1. Frontier progress of foreign research

Foreign research has always maintained a two-wheel drive trend of basic mechanism exploration and engineering technology transformation in the field of integrated circuit reliability, and has made systematic breakthroughs especially in device degradation modeling at advanced process nodes, multi-physics field coupling simulation, and high-frequency testing technology. In the direction of device reliability modeling, aiming at the PBTI effect of 22nm and below FD-SOI transistors under dynamic voltage scaling (DVS) conditions, researchers found that the traditional reaction-diffusion model cannot capture the special phenomenon of "recovery process accelerating subsequent aging" in the stress-recovery cycle. For this reason, a compact model introducing fixed charge saturation effect is proposed, which shows high prediction accuracy under various DVS operation modes and provides a key tool for circuit-level aging analysis [8]. In terms of metal interconnect reliability, as technology nodes shrink leading to continuous rise in current density and continuous tightening of electromigration margins, foreign academia took the lead in promoting the reliability verification paradigm from empirical evaluation based on current density to physical models based on stress evolution calculation, and clearly put forward the forward-looking strategy of "reliability by design", advocating to actively avoid electromigration risks at the layout and routing stage [9].

Research on advanced packaging reliability has become a key investment direction for foreign academia and industry, focusing on failure mechanism analysis under electro-thermal-mechanical multi-physics field coupling [10]. System-level studies show that warpage, interconnect cracking and solder joint fatigue caused by thermal mismatch stress, combined with electromigration and current crowding effects caused by high current density, together constitute the main reliability threats to advanced packaging interconnect structures. Specific failure analysis of fan-out wafer-level packaging shows that its redistribution layer (RDL) structure is prone to various failure modes such as UBM shedding and copper layer tearing under temperature cycling loads [11]. The chemical composition of the failure interface is accurately identified through energy spectrum analysis, which provides direct evidence for clarifying the root cause of failure. In the field of electromagnetic compatibility, in order to break through the 1GHz frequency upper limit of the current IEC standard, foreign countries have developed high-precision broadband probes based on integrated passive device (IPD) technology, extending the conducted EMI measurement bandwidth to more than 20GHz. At the same time, a 3D near-field coupling coil test configuration is proposed to more realistically simulate the electromagnetic environment of multi-chip stacked packages [12]; in addition, by improving the lateral choke structure of the standard stripline cell, the theoretical upper operating frequency limit has been successfully increased by about 16.7% [13].

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In terms of testing technology and talent training, foreign countries have built a complete automated testing system from hardware to software. The solution based on domestic automated test equipment (ATE) integrates Kelvin test, step-by-step method and other technologies to realize efficient verification of the functions and parameters of mixed-signal chips [14]. Particularly noteworthy is that foreign countries have systematically trained reliability professionals with interdisciplinary knowledge by building a curriculum system that connects undergraduate and graduate studies, transforming cutting-edge scientific research results into teaching content in a timely manner, and reserving core strength for continuous technological innovation [15].

2.2. Characteristic breakthroughs of domestic research

While keeping up with international frontiers, domestic research has formed distinct features oriented by engineering application and integrated with multidisciplinary intersection, and has made a number of breakthrough achievements especially in electromagnetic compatibility measurement technology, active optimization of packaging electromagnetic interference, and research on device collaborative failure mechanisms. In the field of measurement technology, aiming at the problem that high-frequency electromagnetic emission signals are weak and difficult to capture, domestic scholars have designed an ultra-wideband active electric probe with a tip width of only 4.1 mm, achieving wideband coverage from 9kHz to 18GHz, with an average gain 15dB higher than that of passive probes, and maintaining a spatial resolution of 0.5 mm at a frequency of 8GHz, which significantly enhances the measurability and accuracy of near-field scanning [16]. At the same time, an enhanced direct power injection test framework based on commercial RF detectors is proposed, which can simultaneously measure the reflection coefficient, impedance, voltage and current at the input end of the device under test, and deeply reveal the internal sensitivity mechanism of the device at different frequency points [17].

In terms of board-level and package-level reliability, China has established a full-link verification system covering from post-silicon manufacturing to terminal applications. Studies point out that chemical, thermal and mechanical stresses introduced by the whole process such as solder paste printing, reflow soldering, and three-proof coating are important causes of chip cracking or solder joint failure. For this reason, various standard methods such as flatness test, warpage monitoring, thermal stress and temperature cycling assessment, and on-line insulation resistance monitoring are integrated to effectively reproduce the failure modes induced by both process and environmental stresses [18]. Aiming at the problem of rapid prediction and suppression of electromagnetic interference in system-in-package, domestic scholars proposed the virtual boundary generalized T-matrix method, which reduces the calculation time from hours to seconds while ensuring 3dB accuracy; further combining this algorithm with deep reinforcement learning, a VBGT-DRL optimization framework is constructed to automatically find the optimal layout scheme under the constraint of limited grounding solder ball resources, reducing the peak value of the package fringe field by about 3.4dB and the peak value of far-field radiation by more than 3dB [19].

In terms of device-level reliability and emerging application protection, China took the lead in systematically studying the synergistic effect of delay faults and BTI aging under FinFET technology [20]. Experimental data show that individual delay faults and individual BTI aging cause 11% and 9.7% delay increments of the reference circuit respectively, but when both coexist, the delay increment is as high as 34.8%. This multiplicative effect will greatly shorten the timing margin of critical paths and cause silent data corruption. In response to the special electromagnetic environment requirements of flexible wearable electronic products, China proposed to build a metal wall isolation structure in the back-end process, reducing the crosstalk of key RF circuits by about

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18.5dB; in the field of electrostatic protection, an ultra-fast response nanoarray protection structure based on phase change materials was developed, and non-pad and internal distributed protection schemes were innovatively proposed, solving the blind spot problem of traditional protection networks in response to internal random discharge.

2.3. Comparison and gap analysis of domestic and foreign research

Through comparison, it can be found that domestic and foreign research presents obvious complementarity in development paths and technical advantages. The core advantages of foreign research are reflected in three aspects: first, in-depth basic physical mechanism research, which can take the lead in discovering new failure phenomena at advanced process nodes and establish accurate physical models; second, mastering the dominance of international standard formulation, and technical specifications in fields such as EMC testing and reliability evaluation methods have global influence; third, the high degree of autonomy of high-end testing equipment and EDA tools has formed a complete technical chain from theoretical research to engineering verification.

The characteristics and advantages of domestic research are concentrated in the field of engineering application implementation and cross-innovation: first, a full-process reliability evaluation system covering chip manufacturing, packaging and assembly to system application has been built, which can quickly solve practical problems faced by the industry; second, it is at the forefront of the integration of artificial intelligence and reliability technology, applying technologies such as deep learning and reinforcement learning to scenarios such as packaging electromagnetic optimization and life prediction, and achieving remarkable results; third, unique technical accumulation has been formed in subdivided fields such as board-level reliability and flexible electronic protection, and some achievements have reached the international advanced level.

At the same time, we must be soberly aware that there are still three obvious gaps in domestic research: first, the basic research on the intrinsic failure mechanism of nanoscale devices is relatively weak, and the microscopic explanation of the nonlinear coupling effect of various aging mechanisms is not in-depth enough; second, high-end reliability testing instruments and simulation tools rely on imports, and core technologies are subject to others; third, there is insufficient voice in the formulation of international standards, and in most cases, we can only passively follow the technical specifications formulated by foreign countries. These gaps are not only the current challenges, but also the key breakthrough directions in the future.

3. Core theories and modeling methods of integrated circuit reliability

3.1. Physics-based failure modeling technology

Physics-based failure modeling is the core foundation of integrated circuit reliability evaluation, which realizes accurate prediction of failure behavior by revealing the internal relationship between material microscopic damage evolution and macroscopic performance degradation. In the field of electrostatic discharge (ESD) modeling, traditional circuit simulation methods are difficult to accurately describe distributed electromagnetic effects under instantaneous high-energy impact. For this reason, researchers have built a hybrid model of full-wave electromagnetic field solver and circuit simulator, integrating three-dimensional full-wave finite-difference time-domain method and circuit simulation technology, and realizing collaborative solution of electromagnetic field and circuit domain through internal ports, which can simulate the transient voltage, current and electromagnetic field distribution of the system under ESD impact with high fidelity [21]. Aiming at

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the unique challenge of charged device model (CDM) protection in 3D chip micro-packaging, an interposer-based distributed ESD protection strategy is proposed, which migrates the ESD protection network from traditional I/O pads to the interposer or near internal charge accumulation nodes, and avoids internal sensitive circuit failure through local discharge paths. Simulation results have confirmed its significant advantage in preventing internal MOSFET breakdown [22].

In terms of thermomechanical fatigue modeling of packaging and interconnect structures, the redistribution layer interconnect structure in fan-out wafer-level packaging will accumulate damage under temperature cycling stress, and its failure modes are diverse, including delamination of under bump metallization (UBM) and copper layer, tearing of solder balls from different interfaces, and fracture of the copper layer itself [11]. In-depth understanding and accurate modeling of these failure modes are the basis for predicting package life and optimizing interconnect geometric parameters and material selection. Process defects during micro-assembly also introduce reliability risks. For example, resin precipitation during curing of epoxy adhesive will contaminate the bonding area and affect the long-term reliability of subsequent interconnections. After analyzing its mechanism through methods such as contact angle measurement, it is found that vacuum baking pretreatment of the substrate surface can effectively remove water vapor and organic impurities, almost completely eliminating resin precipitation, which provides key parameters for process modeling and control [23].

The verification and correction of electromagnetic compatibility models need to fully consider parameter drift caused by environmental stress and device aging. Studies have shown that the model parameters of conducted emission and conducted immunity of integrated circuits are not fixed, but are significantly affected by highly accelerated temperature and humidity stress aging and extreme temperature cycling thermal stress. Aging mainly leads to permanent degradation of active transistor characteristics (such as threshold voltage drift), thereby reducing emission and immunity levels; while thermal stress causes reversible changes in parameters such as impedance of passive distributed networks, and the two work together to change the electromagnetic behavior of the chip [24]. Incorporating aging and thermal stress effects as variables into model parameters can make the model more truly reflect the performance evolution of products in actual service environments, which is particularly important for predictive maintenance in high-reliability application fields.

3.2. Multi-physics field coupling simulation method

With the continuous improvement of integrated circuit integration, single-physics simulation can no longer accurately describe its complex failure mechanism, and electro-thermal-mechanical multi-physics field coupling simulation has become a necessary means to evaluate the reliability of advanced packaging and 3D integrated structures [10]. The multi-physics field coupling simulation framework integrates solvers for electromagnetic field, thermal field and stress field to realize real-time data interaction and iterative calculation between different physical quantities, and can accurately simulate the interaction relationship between current distribution, temperature rise and mechanical stress during device operation. For example, in advanced packaging interconnect structures, Joule heat generated by high current density will cause local temperature rise, which in turn causes thermal expansion of materials to produce mechanical stress, and mechanical stress will change the resistivity of materials and further affect current distribution. This closed-loop coupling effect is the main cause of interconnect failure.

3D integration technology realizes chip stacking through through-silicon vias (TSV) and other methods, which greatly improves the interconnect density, but also brings significant thermal management problems and stress concentration effects. In large-size packages, there is a significant

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mismatch in thermal expansion coefficient between chips, interconnect layers, interposers and substrates of different materials. During power cycling and temperature cycling, repeated thermal stress will continuously accumulate in weak links of the structure, eventually leading to surface deformation, interconnect bump fracture or even body cracking of epoxy molding compound delamination. Multi-physics field coupling simulation can accurately predict the temperature distribution and stress concentration areas in 3D stacked structures, providing a basis for thermal management scheme design and structural optimization.

In the millimeter wave band, electromagnetic-thermal co-simulation becomes particularly important. Design experience of millimeter-wave monolithic integrated circuits shows that due to electromagnetic coupling effects, the electromagnetic simulation results of unit circuits may have huge deviations from traditional circuit-level simulation results, and this difference directly affects the accurate estimation of key indicators such as amplifier gain and output power. At the same time, the high power density of millimeter-wave circuits will cause serious local heating, which in turn affects the electromagnetic characteristics of devices. Therefore, carrying out electromagnetic-thermal co-simulation and combining electromagnetic field solution with heat conduction analysis is a key technology to realize reliable design of millimeter-wave integrated circuits.

3.3. Circuit and system-level reliability design methods

Circuit and system-level reliability design aims to avoid potential failure risks from the design source and ensure the stable performance and function of the chip throughout its life cycle. In high-speed interface design, signal integrity and power integrity are the core considerations of reliability design. In order to achieve broadband low-noise performance in high-speed interfaces, designers usually adopt various bandwidth expansion and noise optimization technologies including coupling peaking inductors. Such designs themselves need to establish accurate parasitic parameter models to ensure that key performances such as bandwidth, gain and noise figure can still meet requirements under process corners and temperature changes [25].

For high-voltage and high-current power integrated circuits, over-temperature and over-current protection are the keys to ensuring their robustness. Corresponding protection circuits require accurate temperature and current sensing models and reliable feedback control mechanisms to ensure that power consumption can be limited in time under abnormal working conditions to avoid permanent damage caused by thermal runaway or electrical overstress. For example, the design of a low-noise power operational amplifier with over-temperature current limiting protection realizes real-time monitoring and protection of the chip's working state by integrating high-precision temperature sensors and current detection circuits [26].

3D integration technology not only brings performance improvement, but also introduces new dimensions of reliability modeling, especially in the intersection of security and reliability. Using the physical characteristics of 3D stacking, chip security can be enhanced at the package level, such as defending against hardware Trojans through split manufacturing, or suppressing electromagnetic information leakage with a metal shielding network embedded in the interposer. However, this complex heterogeneous integration structure also brings new challenges in thermal management, stress distribution and signal integrity. Its reliability modeling must use multi-physics simulation methods to comprehensively analyze the coupling effects between heat, electricity and machinery, so as to evaluate the stability and safety of new packaging structures in long-term operation [27].

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4. Analysis of typical engineering application cases

The value of integrated circuit reliability technology is ultimately reflected in engineering practice. This chapter selects four typical application fields: aerospace, automotive electronics, advanced packaging and intelligent manufacturing, and analyzes the core role and implementation effect of reliability technology in solving practical engineering problems.

4.1. Aerospace field: radiation hardened design of 14nm FinFET devices

Aerospace electronic equipment is exposed to high-energy particle radiation and severe temperature alternation for a long time, and single event effect is the primary factor threatening its reliability. As semiconductor technology enters the 14nm FinFET node, although the three-dimensional gate structure shows stronger radiation resistance by limiting the charge path in the initial stage, its advantages have clear boundaries. Simulation analysis shows that when the linear energy transfer (LET) value exceeds 10 MeV·cm²/mg, the amplitude of the device transient current enters a linear growth interval, and the pulse width widens exponentially. At this time, its radiation vulnerability will be the same as that of planar technology [28].

A more critical finding is that the multi-fin coupling effect caused by ion bombardment position may completely offset the structural advantages. When high-energy particles hit the shallow trench isolation region between double fins, the peak transient current response can be up to five times that of hitting the source-drain region. This finding has completely changed the traditional radiation hardened design idea, indicating that we cannot only rely on the physical characteristics of the FinFET structure itself, but must combine accurate modeling and simulation to identify the most vulnerable sensitive points and design protection circuits accordingly. Based on this, researchers proposed a collaborative strategy of "sensitive area isolation + redundant unit hardening", which reduced the single event upset cross section of the device by an order of magnitude with an area overhead of less than 15%, providing important guidance for the design of aerospace chips at advanced process nodes.

4.2. Automotive electronics field: signal integrity pre-evaluation based on IBIS model

The strict requirements of automotive electronic systems for functional safety make signal integrity the core consideration of reliability design. Traditional design processes often expose problems such as signal reflection and crosstalk at the later physical prototype testing stage, which not only increases R&D costs but also prolongs the product launch cycle. The pre-co-simulation method based on behavioral models provides an effective way to solve this problem.

This method extracts the electrical characteristics of input and output buffers through the IBIS model, combined with electromagnetic field simulation tools to obtain accurate parasitic parameters of the package and interconnect structure, and can comprehensively evaluate potential signal integrity problems at the design stage. The simulation results can not only clearly reveal the signal matching between the driver end and the receiver end, locate the source of signal reflection and crosstalk, but also convert time-domain noise characteristics into frequency-domain conducted emission models to realize quantitative evaluation of electromagnetic interference risks. In the design of a vehicle CAN bus controller, this method was used to detect the overshoot problem on high-speed signal lines in advance. By optimizing the termination resistance value and wiring topology, the signal overshoot amplitude was reduced from 42% to 8%, and at the same time, the

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conducted emission level of the system met the requirements of ISO 11452 standard, achieving a successful design at one time [29].

4.3. Advanced packaging field: thermal cycle reliability optimization of fan-out wafer-level packaging

Fan-out wafer-level packaging (FOWLP), as a key technology for high-density integration, its thermal cycle reliability directly determines the service life of products. With the increase of device power density and the expansion of operating temperature range, the problems of interface stress and structural deformation caused by thermal expansion coefficient mismatch of multilayer heterogeneous materials have become increasingly prominent. For the fan-out package used in a military electronic system, thermal cycle simulation evaluation was carried out through finite element analysis.

The simulation results show that when cycling within the military temperature range of -55℃~125℃, the maximum thermal stress is highly concentrated in geometrically discontinuous and material junction areas such as the interface between the redistribution layer and solder balls, and the peak stress can reach the order of 1.72×10^3 MPa at high temperature stage, becoming the source of fatal failures such as delamination and cracks. At the same time, it is found that the displacement of the packaging material layer is significantly higher than that of internal structures such as chips and micro bumps, and this uncoordinated deformation further aggravates the shear stress at the interface. Based on these findings, researchers optimized from three aspects: first, selecting packaging materials with more matched thermal expansion coefficients; second, designing stress relief grooves in the redistribution layer; third, optimizing the solder ball arrangement. The optimized package structure did not show any failure after 1000 thermal cycles, and its service life was increased by 2.3 times [30].

4.4. Intelligent manufacturing field: full-process reliability guarantee of semiconductor production

The reliability of integrated circuits depends not only on design, but also closely on the manufacturing process. Cluster tools, as the core of semiconductor production lines, their scheduling efficiency directly affects production capacity and product consistency. Inefficient scheduling may introduce defects due to excessive wafer waiting time or improper handling. Facing multiple constraints such as wafer output limits, robotic arm collision prevention, and just-in-time production, traditional heuristic algorithms are difficult to balance solution quality and speed. For this reason, researchers proposed a scheduling method integrating mixed integer programming and hierarchical optimization ideas [31].

This method decomposes the complex global problem into two stages: processing sequence optimization and robotic arm action optimization, and introduces hyperparameters to adaptively adjust constraint conditions, which can complete the solution of high-quality scheduling schemes within seconds to tens of seconds. In the practical application of a 12-inch wafer fab, this method increased equipment utilization by 12% and shortened the average wafer waiting time by 28%, reducing the reliability risk introduced by time factors from the manufacturing process level. At the same time, in the test and verification link, the intelligent test system based on large language model shows great potential. The system can automatically parse data sheets, intelligently recommend test parameters and conduct in-depth error analysis on results, improving test efficiency by more than 40% while reducing the requirements for testers' professional knowledge [32].

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5. Existing technical challenges and bottlenecks

As integrated circuit manufacturing processes continue to scale down to nano and sub-nano scales, the reliability challenges for new ring-gate structure devices and advanced packaging are becoming more severe. Cutting-edge reliability issues have gone beyond the analysis scope of a single failure mechanism, presenting complex characteristics of strong coupling of multiple physics fields and multiple scales, and traditional reliability evaluation methods and design concepts are facing fundamental challenges.

5.1. Device-level reliability challenges

In cutting-edge devices such as nanosheet transistors at the 2nm node, in order to maintain performance and control short-channel effects, the use of ultra-thin high-k dielectric layers and interface layers significantly intensifies the electrical stress on the gate. Although process scaling itself may not introduce new basic failure mechanisms, it greatly increases the occurrence probability and severity of traditional aging effects such as NBTI, PBTI and TDDB. What is more tricky is that there are complex nonlinear coupling effects between various degradation mechanisms. The hot carrier injection effect is particularly complex under advanced nodes, and its interaction with other degradation mechanisms such as NBTI has not been fully clarified. Models of a single mechanism can no longer accurately describe the comprehensive aging trajectory of devices, and the reliability of extrapolating a single experimental result to complex actual working conditions is greatly reduced.

Under FinFET technology, potential defects introduced during manufacturing and device aging during operation will produce nonlinear superposition effects. Experimental data show that when single-fin or multi-fin delay faults that may be missed during wafer factory testing coexist with bias temperature instability, their synergistic effect will lead to a sharp increase in circuit path delay, whose impact far exceeds the simple superposition of individual effects. In the reference circuit, individual delay faults and individual BTI aging cause 11% and 9.7% delay increments respectively, but when both coexist, the delay increment is as high as 34.8%. This multiplicative effect will greatly shorten the timing margin of critical paths, causing the circuit to suffer silent data damage due to timing violations within months rather than years, posing severe challenges to chip design for long-life and high-reliability application scenarios [20].

In addition, tiny process fluctuations and interface defects at the nanoscale are enough to cause significant parameter drift, which in turn affects system performance or even leads to functional failure. The impact of soft errors induced by high-energy particle bombardment on nanoscale low-node capacitance and low operating voltage circuits is becoming more and more prominent, posing a serious threat to high-reliability application fields such as aerospace. The accuracy of transistor-level reliability degradation model transmission to chip and even system level has become the core bottleneck restricting accurate evaluation.

5.2. Package-level reliability challenges

The continuous leap in advanced packaging integration has brought more severe reliability risks while improving system performance. Package-level reliability failures are often the result of the combined action of electrical, thermal and mechanical stresses, whose roots are deeply rooted in the inherent physical mismatch between different materials, bringing great uncertainty to reliability evaluation. Against the background of high-density and heterogeneous integration, signal integrity is

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threatened by multiple factors such as electromagnetic crosstalk, power leakage, and simultaneous switching noise, especially in the millimeter wave band [10].

Design experience of millimeter-wave monolithic integrated circuits shows that due to electromagnetic coupling effects, the electromagnetic simulation results of unit circuits may have huge deviations from traditional circuit-level simulation results. This difference directly affects the accurate estimation of key indicators such as amplifier gain and output power. Without sufficient electromagnetic simulation verification, it may directly lead to tape-out failure. 3D integration technology realizes chip stacking through through-silicon vias and other methods, which greatly improves interconnect density, but also brings significant thermal management problems and stress concentration effects.

In large-size packages, there is a significant mismatch in thermal expansion coefficient between chips, interconnect layers, interposers and substrates of different materials. During power cycling and temperature cycling, repeated thermal stress will continuously accumulate in weak links of the structure, eventually leading to surface deformation, interconnect bump fracture or even body cracking of epoxy molding compound delamination. Some reports point out that in larger-size advanced packaging structures, delamination and cracking defects caused by thermal mismatch may lead to device failure rates as high as 40%. The root cause of reliability failure is evolving from the traditional single stress dominance to a new mode of deep coupling of multiple factors such as packaging process, material properties and system operating conditions [33].

5.3. Limitations of evaluation methods

Accurate evaluation and prediction are the cornerstone of improving integrated circuit reliability. However, existing technical means are still insufficient when facing emerging challenges. Whether it is traditional evaluation methods based on physical failure models or empirical models relying on accelerated life tests, their inherent limitations and complexity make it difficult to achieve both prediction accuracy and efficiency. Traditional accelerated tests take a long time and cost a lot, and it is difficult to simulate the effect of complex stress coupling under real working conditions, and the confidence of their extrapolation results is questionable.

Emerging data-driven methods bring hope for breaking through prediction bottlenecks. By integrating machine learning and intelligent optimization algorithms, they can deeply mine the timing data rules of equipment monitoring and realize accurate estimation of the trend of key degradation parameters. Studies have shown that the long short-term memory network optimized based on the sparrow search algorithm shows significant advantages over traditional manual parameter tuning models in terms of accuracy and generalization ability, with lower root mean square error and prediction curves closer to the real degradation trajectory. However, data-driven methods face problems such as difficulty in obtaining high-quality data and poor model interpretability, and cannot completely replace physics-based modeling methods.

In addition, failures of advanced RF circuits and heterogeneous integrated systems often originate from the strong coupling of electromagnetic field, thermal field and stress field. Existing analysis tools are usually difficult to carry out efficient and accurate full-chip level co-simulation for such complex multi-physics field coupling problems. How to effectively integrate massive online or offline monitoring data, especially integrate information from front-end FEOL and back-end packaging BEOL, to build a unified reliability digital twin prediction platform from transistors to packages is still a core technical problem to be solved urgently [34].

DOI: 10.54254/2755-2721/2026.35296

6. Future development trends and cutting-edge directions

As integrated circuit technology evolves towards finer nodes and 3D integration, the reliability challenges it faces present multi-dimensional composite characteristics, which is driving reliability technology to transform from traditional passive failure avoidance to intelligent active health management and self-repair. Previous studies mainly focused on single-point analysis of specific failure modes and mechanisms, while in the future, it is necessary to build an intelligent system that can deeply integrate multi-physics field feature information and realize real-time decision-making at the same time.

6.1. Intelligent active health management and self-repair technology

Data-driven reliability prediction is the core application direction of intelligent technology. It can establish a dynamic life model by integrating multi-dimensional working condition data such as temperature, stress, radiation load and electromagnetic radiation distribution inside the chip, which greatly improves the prediction accuracy and timeliness compared with traditional methods relying on accelerated life tests. Combining this intelligent sensing capability with closed-loop control gives birth to the concept of a circuit architecture with self-repair potential, that is, through embedded sensors to monitor impedance mutations or specific photoelectromagnetic signals, to locate functional degradation or damaged areas in real time, and trigger preset or dynamically reconfigured redundant units for function replacement or compensation, so as to realize robust maintenance of chip performance during its lifetime. This transformation from post-failure analysis to pre-failure intervention is the fundamental path to cope with increasingly complex application scenarios [34].

The key prerequisite for realizing an intelligent self-healing system lies in a deep understanding of failure physics under extremely complex environments. For example, in radiation protection design for harsh environments such as high temperature and deep space, accurately evaluating the coupling relationship between single event transient effects and voltage and temperature has become the core of ensuring system resilience. Relevant simulation studies show that the adjustment of bias voltage can significantly affect the width and amplitude of transient pulses, which provides a theoretical basis for dynamic voltage regulation to mitigate soft errors. The accuracy of simulation results depends on the accurate modeling of microstructure damage evolution, and the introduction of process miniaturization and 3D stacked structures makes interface characteristics a decisive factor affecting long-term reliability [35]. A study on through-silicon via structures found that temperature cycling will cause microcracks at the insulating layer interface and induce copper diffusion, and its leakage mechanism even undergoes a fundamental change from electrical dominance to mechanical dominance with the number of cycles. Quantitative characterization of such complex degradation behaviors is an indispensable basis for building accurate prediction models [36].

6.2. Multi-scale and multi-physics field fusion simulation technology

Multi-scale reliability simulation integrating materials science, multi-physics simulation and artificial intelligence technology is becoming a cutting-edge tool to reveal the correlation between microscopic failure mechanisms and macroscopic performance degradation. Traditional simulation methods are often limited to a single scale or a single physics field, and it is difficult to accurately describe the complete process from atomic-level defect evolution to system-level functional failure. Future multi-scale simulation technology will realize cross-scale correlation from material atomic structure, device microscopic characteristics to circuit system macroscopic performance, and can

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simultaneously consider the influence of material interface characteristics, process fluctuations and multi-physics field coupling effects on reliability.

The introduction of artificial intelligence technology will significantly improve the efficiency and accuracy of multi-physics field simulation. By training neural networks to replace some time-consuming numerical calculations, the simulation time can be shortened from hours to seconds while ensuring accuracy, which makes it possible to carry out multi-physics field co-simulation at the full chip level. For example, applying deep learning algorithms to the meshing and solving process in electromagnetic simulation can greatly improve the speed of electromagnetic simulation of millimeter-wave circuits and solve the problem of low computational efficiency of traditional methods when dealing with large-scale complex structures.

Building a digital twin platform for integrated circuit reliability is an important development direction in the future. The platform will integrate the whole process data of front-end manufacturing and back-end packaging, establish a unified digital model from transistors to systems, and can map the operating state and degradation process of physical chips in real time. Through the digital twin platform, designers can comprehensively evaluate and optimize the reliability of chips in a virtual environment, and discover potential failure risks in advance, thereby greatly shortening the R&D cycle and reducing trial and error costs [36].

6.3. New protection technology and standardization system construction

Electromagnetic and electrostatic protection in the field of interconnect structures and packaging is another continuously evolving cutting-edge topic, especially in scenarios pursuing higher power density and signal integrity. Studies have found that the near-field magnetic radiation generated by power modules during switching has significant spatial distribution non-uniformity, and the strongest radiation area is often concentrated near the chip close to the DC input terminal, which enlightens us that future electromagnetic compatibility optimization must consider the design paradigm shift of layout sensitivity, from global uniform protection to targeted protection in key areas.

Electrostatic discharge protection also faces new problems caused by scale. As device feature sizes continue to shrink, their sensitivity to static electricity decreases significantly, and traditional centralized protection strategies based on I/O pads are insufficient. Future electrostatic protection technology will develop towards non-pad and internal distributed directions. By directly deploying protection devices at internal circuit nodes, rapid discharge of local charges can be realized, effectively solving the blind spot problem of traditional protection networks in response to internal random discharge. At the same time, combining electrostatic protection with electromagnetic shielding design to build an integrated protection system will become an important means to improve system-level reliability.

Quantifying and controlling the electrostatic level in all links of production and use has become more important than ever. For example, evaluating the risk of charged discharge to sensitive devices by finely measuring the electrostatic state of process equipment and materials, this electrostatic process capability management based on online monitoring is developing towards systematization and digitization, constituting an important part of the reliability guarantee system of intelligent factories. In addition, establishing special reliability evaluation standards and test methods for emerging technologies such as third-generation wide-bandgap semiconductors and 3D heterogeneous integration is also a key task of standardization work in the future [37].

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7. Conclusion

Integrated circuit reliability is the core technology supporting the long-term stable operation of modern electronic systems, and its development is deeply bound to the evolution of semiconductor technology, innovation of integration technology and expansion of application scenarios. This paper systematically reviews the domestic and foreign research progress in the field of integrated circuit reliability from 2022 to 2026, analyzes failure mechanisms, modeling methods and engineering practices from the whole level of devices, circuits, packaging to systems, dissects the current technical bottlenecks, and prospects the future development trends.

Studies show that foreign countries maintain leading advantages in the exploration of intrinsic failure mechanisms of devices at advanced process nodes, the basic theory of multi-physics field coupling simulation, and the formulation of international standards, while domestic countries have formed distinctive features in electromagnetic compatibility measurement technology, cross-innovation of artificial intelligence and reliability, and the construction of board-level full-process evaluation system, and some achievements have reached the international advanced level. Physics-based failure modeling, electro-thermal-mechanical multi-physics field coupling simulation, and circuit-system collaborative design have become the core theoretical support of current reliability technology, and have been successfully applied in fields such as aerospace radiation hardening, automotive electronic signal integrity, advanced packaging thermal cycle optimization, and intelligent manufacturing full-process guarantee.

However, as integrated circuit technology develops towards nodes below 2nm and 3D heterogeneous integration, reliability problems present complex characteristics of strong coupling of multiple physics fields and multiple scales. The nonlinear synergistic effect of various aging mechanisms at the nanoscale, the thermomechanical mismatch problem of large-size advanced packaging, and the limitations of traditional evaluation methods under complex working conditions are still the core challenges to be broken through urgently. In the future, integrated circuit reliability technology will develop towards intelligent active health management, multi-scale multi-physics field fusion simulation, and new integrated protection system. Through the integration of cutting-edge technologies such as artificial intelligence and digital twin, the paradigm shift from passive failure avoidance to active prediction and self-repair will be realized.

The research results of this paper can provide reference for theoretical research and engineering practice in the field of integrated circuit reliability, and are of great significance for promoting the high-quality development of China's semiconductor industry and ensuring the safety of critical infrastructure. Future research should further strengthen the exploration of basic physical mechanisms, break through the core technologies of high-end testing equipment and simulation tools, and enhance China's voice in the formulation of international reliability standards.

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