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Field-Effect Transistors for Logic Integrated Circuits in the post-Moore Era

Ming Jie

Zhengzhou No.11 High School, Zhengzhou, China
hatsuneakira0831@gmail.com

Abstract. As transistor sizes enter the nanoscale, traditional metal-oxide-semiconductor field-effect transistors (MOSFETs) face two fundamental bottlenecks: the short-channel effect and the subthreshold swing limit. In this regard, development in the post-Moore Era has taken two main paths: Firstly, extending Moore's Law through structural innovation—from Fin Field-Effect Transistors (FinFETs) and Gate-All-Around Field-Effect Transistors (GAAFETs) to Complementary Field-Effect Transistors (CFETs)—by utilizing three-dimensional and multi-gate structures to enhance gate control capabilities and effectively mitigate the short-channel effect; Second, seeking breakthroughs through physical mechanisms and materials, such as Ferroelectric Field-Effect Transistors (FeFETs) using negative capacitance effects, Tunneling Field-Effect Transistors (TFETs) based on quantum tunneling, and Two-Dimensional Field-Effect Transistors (2D FETs) with single-atom-thick channels, aimed at overcoming subthreshold swing limitations and achieving ultra-low power consumption. Currently, structural miniaturization has reached the limits of manufacturing processes and thermal management, while devices based on new physical principles still face challenges in terms of reliability and integration. Future trends will move beyond a single dimension toward the collaboration and integration of structure, physics, and materials, collectively driving the evolution of integrated circuits.

Keywords: post-Moore Era, subthreshold swing, short-channel effect, structural miniaturization, field-effect transistor

1. Introduction

The progress of integrated circuits since the 1960s has been in line with the forecasts of Moore's Law. The industry has realized exponential performance and integration density by relentlessly shrinking the feature size of transistors through scaling of the process. At the micrometer scale, actually reducing the size of devices can be effective in enhancing performance, which has led to the further development of the industry [1]. But below the 22-nm node, the further scaling of MOSFETs is limited by two basic physical bottlenecks. The first is the short-channel effect: the capability of the gate to regulate the channel reduces drastically with a reduction in dimensions and causes a spike in leakage current. The traditional method of improving performance through miniaturization alone is harshly curtailed by the resulting power wall as the transistor density gets higher. Then comes the so-called Boltzmann limit: the conventional switching mechanism, which relies on thermionic

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emission, places a theoretical lower limit of about 60 mV/dec on the subthreshold swing (SS) and is the real limit to further operating voltages and power savings. These two significant bottlenecks are precisely what have rendered it challenging to continue with Moore's Law, which is based upon the miniaturization of traditional processes.

In this case, semiconductor technology has reached the post-Moore Era. To counter these challenges, the industry and academia have designed two fundamental solutions: First, by designing device structures to extend Moore's Law. As an example, FinFET and GAAFET, already in mass production, by placing the gate around the channel on three or four sides the gate control is greatly enhanced, and the short-channel effect is suppressed. The CFET now being developed is designed to be as area-efficient as possible by stacking n-type and p-type devices vertically. Nevertheless, traditional operating principles have not been changed and such devices, which operate using structural miniaturization, cannot overcome the theoretical limit of subthreshold swing. Second, by innovating physical mechanisms and materials to transcend Moore's Law, scientists aim to fundamentally revolutionize traditional switching mechanisms. An example is FeFET, which uses the negative capacitance effect to amplify the gate voltage, and TFET, which uses quantum tunneling mechanisms to replace thermal emission; both should overcome the subthreshold swing limitation; and 2D FET enhances electrostatic control at the material level and suppresses the short-channel effect thanks to its atomically thin channels.

This paper will systematically discuss the above two development paths following the chronological order of FET development from the past to the future as shown in Figure 1. By concentrating on overcoming the short-channel effect and subthreshold swing, this paper will engage in a comparative analysis of the advantages, disadvantages, and complements of the different types of devices. Chapter 2, gives a brief background of the operating principles and physical constraints of traditional MOSFETs, explaining what the next generation device should aim to achieve. Chapter 3 will discuss the structural development of mainstream devices that are already in mass production (FinFETs and GAAFETs) and the energy efficiency bottlenecks. Chapter 4 dwells on the leading-edge devices (CFET, FeFET, TFET, and 2D FET) and their operating principles, their strengths, and weaknesses, and unlocks their possibilities of technological convergence by comparison. Lastly, Chapter 5 concludes on the history of development and sketches the future orientation in the progress of integrated circuits with multidimensional collaborative innovation of structure, mechanisms, and materials.

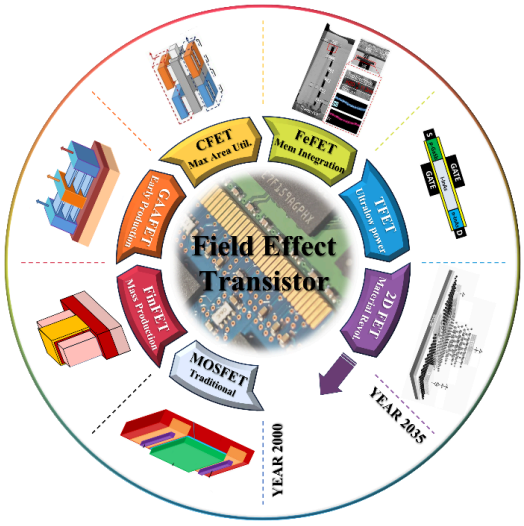


Figure 1. Evolution of FETs from past to future [2-6]

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2. A brief overview of the principles of field-effect transistors

A traditional metal-oxide-semiconductor field-effect transistor (MOSFET) is an electronic device that uses a gate electric field to control the switching of current; its basic structure consists of a gate (G), a drain (D), a source (S), and a channel. Taking an NMOS transistor as an example, one can form two heavily doped n^+ regions (source and drain) on a p-type substrate. When a sufficiently high positive voltage is applied to the gate, an inversion layer is induced on the semiconductor surface beneath the gate oxide, forming a conductive channel that connects the source and drain [2]. MOSFETs utilize this principle to achieve switching control, and this operating mechanism was also adopted by FinFETs, GAAFETs, and CFETs in the early post-Moore Era.

As MOSFET device dimensions shrink, they face limitations imposed by two fundamental physical principles. The first is the theoretical limit of the subthreshold swing [3]. The subthreshold swing (SS) is defined as the change in gate voltage required to produce a one-order-of-magnitude change in source-drain current, that is:

$$\mathrm{SS}=\frac{\mathrm{dV_{gs}}}{\mathrm{d}(log_{10}I_d)} \tag{1}$$

In particular, the differential relationship between the gate voltage V_{gs} and the surface potential φ can be derived from the principle of voltage division across a capacitor. The drain current I_d is generated mainly through diffusion mechanisms; it is proportional to the carrier concentration, and the relationship between I_d and the surface potential φ can be obtained from the Boltzmann distribution:

$$\frac{\mathrm{d}\varphi}{\mathrm{dV_{gs}}}=\frac{\mathrm{C_{ox}}}{\mathrm{C_{ox}+C_d}} \tag{2}$$

$$\mathrm{I_d}\propto\exp\left(\frac{\mathrm{q}\varphi}{\mathrm{kT}}\right) \tag{3}$$

Consider the case where the gate can perfectly control the channel, i.e., $C_{ox} \gg C_d$ (at room temperature, 300 K)

$$\mathrm{SS}=\frac{\mathrm{dV_{gs}}}{\mathrm{d}\varphi}\frac{\mathrm{d}\varphi}{\mathrm{d}(\log_{10}\mathrm{I_d})}=\ln(10)\cdot\frac{\mathrm{kT}}{\mathrm{q}}\approx 60\ \mathrm{mV} \tag{4}$$

This means that, based on the conventional switching mechanism of thermionic emission, the gate voltage must change by at least 60 mV to reduce the current by an order of magnitude—this is known as the "Boltzmann limit," which fundamentally limits further reductions in operating voltage and power consumption. The second factor is the short-channel effect. When the channel length is small enough, the potentials at the source and drain interfere with the gate's control over the channel, causing the source-drain potential barrier to decrease and the leakage current to increase. An approximate solution for the leakage current I_{leak} can be obtained using the Boltzmann distribution and the Poisson equation:

$$I_{leak}\approx I_0\cdot exp\left(\frac{\Delta\varphi_{DIBL}}{kT/q}\right)\approx exp\left[\frac{V_{ds}+\varphi_{bi}}{kT/q}\cdot exp\left(-\frac{L}{\lambda}\right)\right] \tag{5}$$

The leakage current I_{leak} increases at a double-exponential rate as the channel length L decreases, making it difficult to further scale traditional MOSFETs below the 22-nm node.

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To conclude, the short-channel effect and subthreshold swing limit are the two primary limitations impeding further scaling of conventional MOSFETs. The former leads to poor gate control as devices are miniaturized, causing higher static power. The latter results in a subthreshold swing of 60 mV/decade and caps the reduction of dynamic power. These bottlenecks set the primary focus for device research in the post-Moore Era: to suppress short-channel effects and to break the subthreshold swing limit.

3. Innovations in structural miniaturization

Miniaturization of traditional MOSFETs has reached its limitations at the 22 nm process node and below. Consequently, the industry has looked to radical structural innovations to extend Moore's Law. The primary technique involves a shift from a two-dimensional design to a three-dimensional design, thus increasing the number of gate surfaces that surround the channel and regaining control over the short-channel effect.

3.1. FinFET

When the scaling of planar MOSFETs hit a wall around the 22-nm node due to the short-channel effect, FinFETs were invented [4]. The main innovation is to make the channel a vertical fin-shaped and make the gate go around the fin on three sides. This three-dimensional construction greatly enhances the area of contact between the channel and the gate, which will allow to shield more efficiently the interference between the source and drain potentials. Consequently, although the channel length keeps on reducing, short-channel effects are maintained within a manageable territory. This has also enabled FinFET to be the prevailing technology, and has resulted in its use being prevalent, before the 3-nm node [7]. What has made FinFET successful is that, without changing the basic operating principle of the traditional MOSFETs (i.e., the process of thermal electron emission), it successfully solved the most pressing bottleneck, namely, the short-channel effect, by a structure revolution between planar and three-dimensional designs, with only slight modification to the existing industrial ecosystem in terms of manufacturing processes.

Yet, it is exactly the fact that FinFETs do not change the principles of their operation that cannot allow them to overcome the theoretical limit of 60 mV/dec of subthreshold swing. Moreover, with the shrinkage of process nodes to less than 5 nm, FinFET fin miniaturization is nearing physical constraints and quantum tunneling effects are becoming more dominant, and it is becoming harder to continue to improve performance. This implies that the use of the FinFET architecture evolution is no longer adequate to address the needs of additional scaling.

3.2. GAAFET

Gate-All-Around Field-Effect Transistors (GAAFETs) represent a logical evolution on the structural miniaturization path. New electrical variability problems lie in the increase of FinFET fins when they grow taller and thinner in order to reach higher drive currents. GAAFET is able to produce a gate-all-around structure enveloping the channel on every side of the channel by converting the channel into horizontally stacked nanosheets (or nanowires). Its benefits are mostly seen in the 3 pillars namely; Firstly, the fully enclosed gate offers the most effective electrostatic control to date, further removing short-channel effects; Secondly, the channel width (i.e. the width and number of nanostrips) can be flexibly designed allowing an optimum trade-off between drive current and area; Thirdly, its three-dimensional stacking capability enables higher device density within the same

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occupied area, thereby increasing integration density [7]. Nonetheless, GAAFETs are also based on conventional working principles and have not been able to break through the subthreshold swing limit. Meanwhile, with its complex nanosheet stacking architecture, it demands unparalleled precision demands of manufacturability (uniformity of gates and stress control), and the heat dissipation challenges of high-density integration are rapidly getting worse [4].

3.3. From finfet to GAAFET

The shift from single-gate planar to multiple-gate three-dimensional devices is the key to sustaining Moore's Law in the early post-Moore Era [1]. In fact, the increase in the number of gates around the channel—from a single side in planar MOSFETs to three sides with FinFETs and then four sides for GAAFETs—represents an obvious technological evolution that attempts to defeat the short-channel effect by increasing electrostatic control. While 3D structures have considerably added to manufacturing complexity, it is precisely these structural innovations that have enabled Moore's Law to extend to the 3 nm node and beyond.

But as illustrated in Table 1, such developments from planar MOSFETs to FinFETs and to GAAFETs are united under the same technological paradigm: namely, stepwise advances based on the metal-oxide-semiconductor (MOS) operating mechanism. And, whilst they certainly solved the short-channel problem quite well, they never challenged thermionic emission as a switching mechanism. As a result, the Boltzmann limit for subthreshold swing (60 mV/dec) is an intrinsic barrier for any additional decrease in operating voltage and power consumption. This implies that pure structural miniaturization has intrinsic limitations in energy efficiency improvement, which calls for a fundamental change in operating principles.

Table 1. Comparison of mainstream FET evolution

Device Type	Core Iteration Logic	Gate Surfaces	Representative Technology Node	Key Advantages	Main Challenges	Breakthrough of SS Limit
Planar MOSFET	/	1	＞22 nm	Principle and process foundation	Severe short-channel effects	No
FinFET	Planar → 3D	3	22 nm-3 nm	Better electrostatic control	Gain bottleneck below 5 nm	No
GAAFET	Increase gate count	4	＜3 nm	Optimal electrostatic control, adjustable current	Complex process, heat dissipation challenges	No

4. Device innovation beyond traditional paradigms

Semiconductor technology is today in a critical milestone in development of GAAFET to next generation architecture. With the 3D devices nearing their limit in terms of manufacturing technology and power consumption, frontier research has split off in two directions based around two key goals: First, extending 3D integration to its furthest point, to keep on reducing device density, as with CFETs; Second, radically re-evaluating the switching mechanisms to eliminate bottlenecks in energy efficiency, such as FeFETs and TFETs. The 2D FETs have become a perfect material platform to facilitate the two approaches in part due to their atomic-scale thickness and high-quality properties.

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4.1. The ultimate extension structural miniaturization

The final implementation of the structural miniaturization approach is complementary field-effect transistors (CFETs). Its fundamental innovation is to vertically integrate NMOS and PMOS devices, which are normally placed side by side, and therefore attain a radical reduction in the area of logic cells on a two-dimensional plane.

The gigantic density advantage of CFET is accompanied by manufacturing and reliability problems that have never been witnessed previously. The high complexity of the manufacturing process is first and foremost. At such scales, the precision of vertical registration between upper and lower transistors is required to be very high; a single nanometer variation can result in device failure, making photolithography and etching technologies extremely challenging. Following is the grave problem of self-heating. The stacking architecture has three-dimensional structure that greatly impedes the heat transfer path to the substrate, leading to a dramatic increase in the local device temperatures. This does not only impact performance and reliability but may also cause timing errors in the circuits.

The academic and industrial community is striving to seek solutions to these challenges. Sequential CFETs (where the underlying devices are made, and then the top layer is grown epitaxially) and monolithic CFETs (where both are made in a single step on a single wafer) have their own merits and demerits in terms of integration methods: the former has design flexibility but is limited by thermal budget constraints on the underlying devices, whereas the latter is cost-effective but very difficult to integrate processes [8]. Thermal management in thermal management research, it has been found that the self-heating effect in CFETs can also raise the read and write delay of SRAM cells by almost 10 percent [9]. In response to this, designs have been suggested like buried thermal rails, which would offer a rapid conduit to heat, which is trapped in the stacked layers and can greatly lower thermal resistance, and slightly improve performance [5].

CFET takes the idea of reducing three-dimensional structures to the extreme physical limits and at the same time exerts the maximum pressures on manufacturing and maximizing the resulting manufacturing and thermal management challenges. This has given rise to the fact that at an atomistic level, it is becoming more challenging to solely depend on structural innovations. Scientists need to revolutionize the switching mechanisms in order to overcome the barrier in power consumption.

4.2. Innovations in physical mechanisms

In contrast to CFETs, which explore perfection within existing paradigms, another innovative initiative defines itself by innovation at the level of physical principles. Through new mechanisms or materials, Scientists seek to fundamentally break the Boltzmann limit of energy loss associated with subthreshold swing (SS) and resolve the energy efficiency bottleneck that cannot be addressed through structural miniaturization alone.

4.2.1. Negative capacitance effect device

The fundamental novelty of ferroelectric field-effect transistors (FeFETs) is the introduction of ferroelectric materials into the gate stack. Internal gate voltage amplification with the negative capacitance effect of the material is theoretically achievable with a subthreshold swing of less than 60 mV/decade, making the device potentially capable of ultra-low-voltage switching [2]. Moreover, non-volatile polarization characteristics of the ferroelectric materials give them an inherent

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compatibility with the memory cells, which can create perfect device platform to construct energy efficient in-memory computing architectures.

The main problem of commercialization of FeFETs is, however, the reliability and longevity of the ferroelectric materials. Ferroelectrics have fatigue and aging following repeated switching resulting in narrowing of the storage window and performance deterioration, hence limiting their use as logic devices [6].

In spite of this, FeFETs have shown immense potential in experimental investigations. At the device scale, FeFETs with gate lengths of sub-5 nm and made with van der Waals heterojunctions have obtained an incredibly low subthreshold swing of 6.1 mV/decade at room temperature, much smaller than usual limits [2]. On the system application level, an in-memory computing macrocell fabricated using FeFETs with built-in ferroelectric capacitors implemented via backend process integration had a peak power efficiency of up to 171.34 TOPS/W, and a cycle capacity of over 107 cycles, demonstrating its practicality in the application of AI edge computing [6]. These advances suggest that FeFETs are simultaneously developing in two different directions: to ultra-low-power logic switches, and to new computing paradigms.

4.2.2. Quantum tunneling devices

Unlike traditional FETs that depend on thermal electron emission, TFET employs the quantum-mechanical interband tunneling effect for carrier injection. As a result, TFET could have a subthreshold swing that is not limited by the 60 mV/dec thermodynamic limit. This tunneling effect may help TFETs have a much lower off-current and operating voltage. There is a high possibility that TFETs can help resolve issues associated with energy efficiency.

The biggest challenge with TFET design is the lack of control over defects/impurities that increase the tunneling barrier, which decreases the steep switching characteristics. This results in low ON current and high subthreshold swing [2]. Hence, the identification of materials with optimum bandgap and junctions with atomic sharpness is of importance.

Recently, some breakthroughs have been seen in TFET materials and devices. For TFET devices with the same targets as traditional CMOS devices, theoretical modeling showed that TFETs would require less power. Experimental results are even more promising [2]. For the first time, two-dimensional materials Tl_2O based TFETs showed high performance and excellent power efficiency with a conduction current of 3449 μA/μm, subthreshold swing of 49 mV/dec and gate length of 10 nm. This is a significant milestone in the development of TFET and high-performance low power devices [10].

4.3. The search for ideal materials

Two-dimensional field-effect transistors (2D FETs) are a new frontier in channel materials. Semiconductors with two dimensions (MoS_2 and WS_2) have atomically thin layers (usually a single layer or a few layers). The two main benefits of this property are: First, its atomic-scale thickness allows electrostatic control of the channel potential near-perfectly with inherent resistance to the short-channel effect at the underlying physical scale [3]. Second, and more to the point, two-dimensional materials, themselves, can be a perfect material platform. Their atomically smooth surfaces, which do not contain any dangling bonds, facilitate their combinations with heterogeneous materials like dielectric gates, which opens opportunities to the creation of new devices like high-performance two-dimensional negative-capacitance FETs.

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Nevertheless, the implementation of 2D FETs on a practical basis continues to be challenged on a basic level, in terms of materials, interfaces, and integration [1]. Firstly, the problem of ensuring a high-quality and wafer-scale monocrystalline thin film is a challenge. Secondly, the extremely large contact resistance between the metal and the two-dimensional semiconductor severely constrains the drive current. Thirdly, the two-dimensional surface of materials is highly sensitive to external environment (adsorbed species and interfacial trap states) which influence device stability and uniformity in performance. The core of these issues is that atomic-scale channels make the impact of material defects, interfacial disorder, or doping oscillations enormous.

Considerable advances have been achieved on the most basic issues of material preparation and doping. As a case in point, Hou et al. have created a metal-assisted van der Waals epitaxy, in which they managed to grow single-layer MoS_2 uniformly at the wafer scale, and controllable substitution doping on this platform was first demonstrated: P-type doping was done with Nb, Cu, and V, and n-type doping was done with Fe, which yielded a mobility as high as 71.2 $cm^2/V \cdot s$ and an on/off ratio of 10^8 [11]. This publication offers a critical technological groundwork towards overcoming the problems of large-scale integration and circuit application of 2D FETs.

4.4. Horizontal comparison and prospects for integration

Each of these four advanced FETs has its own distinct features regarding the principles, benefits and obstacles. CFETs further extend the structural miniaturization concept, pushing to density limits but unable to overcome energy efficiency scaling issues; FeFETs and TFETs, based on negative capacitance and tunneling respectively, can overcome SS scaling, but cannot resolve reliability problems and sensitivity to non-ideal effects; 2D FETs, as a material platform, can be paired with the other technologies listed above. Table 2 clearly shows that each of the four cutting-edge technological pathways described above has its own distinct characteristics and limitations. However, the comprehensive requirements for integrated circuit performance in the post-Moore Era —which call for higher density, lower power consumption, and potentially new functionalities— make it difficult for any single approach to meet these demands on its own.

The key to future breakthroughs lies precisely in taking the initiative to break down the barriers between the structures, mechanisms, and materials presented in the table, and moving toward "purposeful synergy and integration" among them. This trend is no longer mere speculation but is rooted in current cutting-edge research: for example, by combining the platform characteristics of two-dimensional materials with either the negative capacitance effect or quantum tunneling mechanisms, it is possible to simultaneously achieve optimal electrostatic control and steep switching characteristics, or high drive current and low subthreshold swing; The structural concept of employing the layered nature of two-dimensional materials to achieve three-dimensional stacking has led to the development of 2D CFETs, which are designed for extreme integration density [12]; Going a step beyond, attempts have been made to achieve cross-paradigm coupling at the level of physical mechanisms, such as integrating negative capacitance with quantum tunneling into a single device; this could even lead to the development of novel-principle devices that combine ultra-low power consumption with rich analog signal processing capabilities [13].

These explorations collectively point to a future that transcends the current landscape of competition: the paradigm of transistor development is evolving from a linear progression along a single mainstream technological path to a systematic engineering approach that involves collaborative design and innovation across three dimensions—structure, physical mechanisms, and materials systems.

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Table 2. Comparison of emerging field-effect transistors

Device Type	Concept and Working Principle	Key Advantages	Main Challenges	Technology Readiness	Breakthrough of SS Limit?
CFET	Structural scaling	Area efficiency improved; compatible with existing CMOS process	Severe self-heating effect extremely high alignment precision required;	R&D stage; TSMC targets mass production in the 2030s	No
FeFET	Negative capacitance effect	SS below 6.1 mV/dec [2]; in-memory computing	Ferroelectric material fatigue; memory window degradation with cycling	Lab stage; in-memory computing macro has been taped out [6]	Yes
TFET	quantum mechanism	SS below 60 mV/dec; ultra-low static power; 2D TFET achieves high on-current of 3449 μA/μm [10]	On-current lower than MOSFET; ambipolar leakage issue	Lab stage; some material systems approaching practical application [2, 10]	Yes
2D FET	Atomic-scale channel material	Inherent immunity to short-channel effects [3]; potential for flexible applications	crystal growth challenging; high contact resistance; sensitive to interface traps [1]	Lab stage; breakthroughs in wafer-scale integration [11]	Depends on integration mechanism

5. Conclusion

The development of field-effect transistors in the post-Moore Era has clearly taken two distinct paths: one that "continues" Moore's Law and another that "transcends" it. The path to "continuation" lies in radical innovation at the structural level. From FinFETs and GAAFETs to CFETs, three-dimensional integration and gate dimension scaling have been used to maintain gate control capabilities and density scaling; however, due to the limitations of thermal emission, improvements in energy efficiency are nearing a bottleneck. The way towards transcendence is based on the radical shifts in physical principles and materials. By taking advantage of the negative capacitance effect and quantum tunneling respectively, FeFETs and TFETs have in principle broken the Boltzmann limit on subthreshold swing; 2D FETs, whose channels are atomically-sized, provide an ideal platform in which the electrostatic control and heterogeneous integration can be achieved.

The future opportunities do not consist in a two-choice, but in the profound synthesis of these three directions. New mechanisms (2D-FeFET, 2D-TFET), new structures (2D-CFET), can be combined with the two-dimensional materials platform to coordinate performance improvement; cross-integration between mechanisms (e.g. Fe-TFET) can even be done, resulting in the development of groundbreaking devices that can combine ultra-low power consumption and new capabilities. This is a change in the transistor development paradigm, where single-scale miniaturization is supplanted by multidimensional, collaborative design, bringing together structure, mechanisms, and materials.

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In the direction of more practical applications, various use cases will lead to the heterogeneous integration of components heterogeneously: Mobile devices may consider using energy-efficient devices based on new mechanisms, like using FeFETs based on 2D technology in office laptops to vastly increase battery life; high-performance computing may integrate the high-density engineering with new mechanisms to achieve the best performance. For example, desktop computers could utilize Fe-CFETs to power up multi-core computing and pursue peak performance to achieve this vision, it is high time to come up with new integrated technologies, design methodologies, and EDA tools that can help in fulfilling these demands. Consequently, the horizon of innovation in integrated circuits has been greatly broadened and a new dawn is rising, where multidimensional collaborative innovation will create unending development in computing power and energy efficiency.

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