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Parameter-Scanning Analysis of a Single-Phase Full-Bridge Rectifier with Capacitive Filtering: Trade-Off Between Ripple Suppression and Current Stress

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Abstract. A single-phase full-bridge rectifier followed by a filter capacitor is a basic front-end structure in low-voltage DC supplies, auxiliary power units, and small power converters. A larger filter capacitor usually reduces the DC-side voltage ripple, but it also shifts diode conduction toward the peaks of the AC voltage and concentrates the charging current in a shorter time interval, increasing peak current and thermal loading in the rectifier bridge. To quantify the coupling between output-voltage quality and device current stress, this paper develops a continuous-time simulation model of a single-phase full-bridge rectifier with capacitive filtering, including diode forward voltage drop and source-side equivalent series resistance. Five capacitance values and three load resistances are scanned. Under a 50 Ω load, increasing the filter capacitance from 220 μF to 4700 μF raises the average DC voltage from 241.84 V to 283.00 V and reduces the ripple factor from 0.1751 to 0.0098. At the same time, the reported diode charging-current peak increases from 19.17 A to 32.42 A, the RMS value increases from 8.36 A to 12.08 A, and the conduction angle per charging pulse decreases from 74.33° to 47.03°. Under the 20 Ω heavy-load case, the peak current reaches 56.62 A, showing that heavy loading amplifies the current-stress penalty of large capacitive filtering. A ripple-factor versus peak-current trade-off curve further shows that capacitance selection should consider output ripple, load level, and rectifier current margin simultaneously, rather than minimizing ripple alone.

Keywords: single-phase full-bridge rectifier, capacitive filtering, parameter scanning, ripple factor, conduction angle

1. Introduction

Rectification and DC-link filtering are common front-end stages in power electronic converters. The single-phase full-bridge rectifier remains widely used in auxiliary supplies, low-voltage DC supplies, charger front ends, and small industrial power supplies because of its simple structure, low cost, and no control requirement [1, 2]. In this circuit, bridge rectification only changes the voltage polarity; a low-frequency pulsating component remains at the output. If the following load or control stage is directly exposed to this pulsating voltage, voltage stability, device loss, and control margin may all be affected. A shunt capacitor is therefore often used to support the DC link by storing

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energy near the voltage peak and releasing it after the peak. The capacitance, however, cannot be selected from the ripple requirement alone. It also affects rectifier current stress, thermal design, start-up inrush, volume, and cost.

Diode-rectifier modeling and harmonic analysis have been studied extensively. Drapela et al. [3] developed an analytical model of a single-phase diode bridge rectifier under supply-voltage interharmonics to explain the harmonic and interharmonic distortion produced by the rectifier. Their model improves the description of source-side distortion, but it mainly supports grid-side harmonic assessment and pays less attention to the device-current stress caused by filter-capacitor variation. Busatto et al. [4] compared several models of single-phase diode bridge rectifiers for harmonic studies with many devices, focusing on model accuracy, computational cost, and system-level simulation efficiency. Their work addresses large-scale harmonic analysis, but does not jointly evaluate output ripple, diode charging-current peak, RMS current, and conduction angle for capacitance selection. These studies show that the nonlinear conduction of a diode rectifier strongly shapes the current waveform, while most existing discussions remain centered on power quality or equivalent modeling.

A second group of studies improves rectifier-front-end performance through topology and control. Miletic and Grbović [5] designed a single-phase half-bridge rectifier with an active DC bus to improve DC-side energy exchange and operating performance. Abbas et al. [6] proposed a diode rectifier assisted by a series-connected chopper to reduce input-current total harmonic distortion. Israr and Samuel [7] studied a front-end PFC controller with a small DC-link capacitor for light electric-vehicle chargers, reducing the influence of a low-bandwidth voltage loop on current quality. Wei et al. [8] used active power decoupling to suppress double-line-frequency power ripple in a single-phase system. van der Broocke Campos et al. [9] adopted a hybrid switched-capacitor PFC boost rectifier to reduce the required voltage gain. These methods can improve power factor, DC-link ripple, or dynamic performance, but they generally require additional switches, controllers, or power-decoupling units. In many low-cost and low-complexity applications, the diode bridge with a shunt capacitor remains the more practical option; its parameter-selection boundary therefore still deserves closer analysis.

Capacitor reliability and filter-parameter selection have also been examined. Yamasoto and Hasegawa [10] studied condition monitoring of a DC-link capacitor in an inverter with a front-end diode rectifier under imbalanced three-phase supply, showing that capacitor degradation directly affects inverter reliability. Li and Du [11] used a virtual-impedance strategy to suppress double-line-frequency ripple at the input side of a micro-inverter. Hu and Ma [12] analyzed typical filter-capacitor faults in an auxiliary power-unit inverter. Tan [13] discussed the influence of filter-capacitor selection on the operating time of non-full-phase protection relays. These studies show that the filter capacitor is not only an energy-storage element; it also affects output quality, device stress, and operating constraints. However, existing work is often directed either toward complex topologies and active control or toward capacitor fault diagnosis. The coupled variation of ripple, charging-current stress, and conduction angle in the basic single-phase full-bridge rectifier with capacitive filtering remains insufficiently quantified.

Therefore, this study focuses on the quantitative performance evaluation of the conventional single-phase full-bridge rectifier with capacitive filtering, rather than on a topological redesign. By constructing a reproducible parameter-sweeping procedure, the average DC voltage, ripple factor, diode charging-current peak, RMS current, and single-pulse conduction angle are simultaneously extracted under different combinations of capacitance and load resistance, enabling a comprehensive assessment of the coupling between filtering performance and device current stress. The main

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contributions are as follows: 1) a continuous-time rectifier-filter simulation procedure is constructed with diode forward voltage drop and equivalent series resistance, so that the conduction threshold and finite charging-current amplitude can be explicitly represented; 2) a multi-index evaluation framework covering output quality, current stress, and conduction-time distribution is adopted; 3) the coupling among capacitance, load level, and current stress is quantified using fifteen capacitance-load combinations; and 4) a ripple-factor versus peak-current curve is used to indicate the engineering trade-off boundary in capacitance selection.

2. System model and parameter-scanning method

2.1. Equivalent model of the rectifier with capacitive filtering

The studied circuit consists of a single-phase AC source, a full-bridge diode rectifier, a shunt filter capacitor, and a resistive load. To support parameter scanning and metric extraction, a continuous-time equivalent model is used without introducing the detailed switching behavior of a specific diode device. The core relationships are:

$$v_s(t) = V_m sin(\omega t), \qquad \omega = 2\pi f \tag{1}$$

$$v_r(t) = |v_s(t)| \tag{2}$$

$$i_D(t) = max\left(\frac{v_r(t) - v_c(t) - 2V_D}{R_s}, 0\right) \tag{3}$$

$$\frac{\mathrm{d}v_c(t)}{\mathrm{d}t} = \frac{i_D(t) - \frac{v_c(t)}{R_L}}{C} \tag{4}$$

where $v_s(t)$ is the AC input voltage, $v_r(t)$ is the full-wave rectified voltage, $i_D(t)$ is the charging current flowing through the conducting diode pair of the bridge rectifier, and $v_C(t)$ is the filter-capacitor voltage, namely the DC output voltage. V_m denotes the peak value of the AC input, ω is the angular frequency, t is time, V_D is the forward voltage drop of one diode, R_s is the source-side equivalent series resistance, C is the filter capacitance, and R_L is the load resistance. The max(·) function ensures that the charging current is nonnegative.

The above equations describe, in sequence, the AC input voltage, the full-wave rectified voltage, the charging current limited by the conduction threshold and loop resistance, and the dynamic variation of the capacitor voltage. Since two diodes conduct in each charging path of the bridge, the conduction threshold includes twice the forward voltage drop of one diode. The max(·) function represents the unidirectional conduction characteristic: the charging branch is blocked when the rectified voltage is lower than the capacitor voltage plus the diode drops, and the capacitor is charged when this threshold is exceeded. The model retains the three key factors of capacitor charging and discharging, conduction threshold, and source-resistance current limitation, and can therefore represent the pulsed-charging behavior of a capacitor-input rectifier.

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To make the subsequent metric extraction reproducible, the above relationships are implemented in Simulink, as shown in Fig. 1. The model includes the AC input, full-wave rectification, conduction-threshold judgment, series-resistance current limiting, capacitor integration, and load-discharge branch. Measurement ports are set for the AC voltage, rectified voltage, charging current, and DC output voltage.

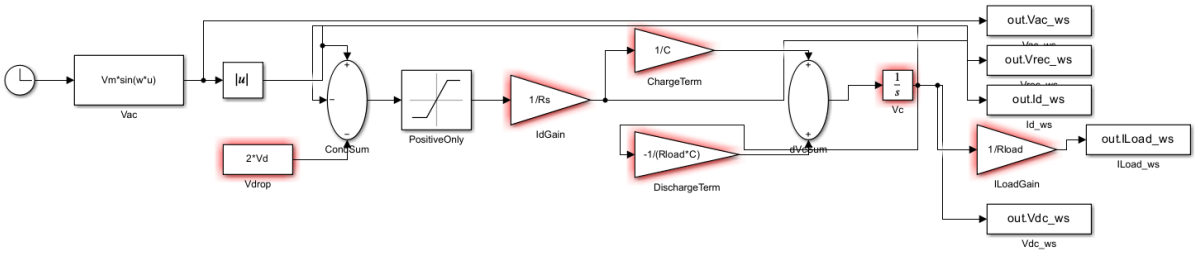

Figure 1. Equivalent Simulink model of the single-phase full-bridge rectifier with capacitive filtering

2.2. Parameter settings and evaluation indices

The parameter scan is conducted under the same AC input condition to ensure comparability among different operating cases. Table 1 lists the main simulation parameters. The filter capacitance ranges from 220 μF to 4700 μF, covering typical conditions from weak filtering to strong filtering. The load resistance is set to 20 Ω, 50 Ω, and 100 Ω, representing heavy, medium, and light load conditions, respectively.

Table 1. Basic simulation parameters

Parameter	Symbol	Value
AC voltage peak value	V_m	311 V
Line frequency	f	50 Hz
Angular frequency	ω	2πf
Forward drop of one diode	V_D	0.85 V
Equivalent series resistance	R_s	0.8 Ω
Filter capacitance	C	220, 470, 1000, 2200, and 4700 μF
Load resistance	R_L	20, 50, and 100 Ω
Simulation time	t_{stop}	0.30 s
Initial capacitor voltage	V_{C0}	0 V

The evaluation indices are selected from three aspects: output quality, device current stress, and conduction-time distribution. The average DC voltage and ripple factor characterize the DC output quality; the diode charging-current peak and RMS value represent instantaneous current impact and equivalent thermal loading, respectively; and the conduction angle describes the time distribution of the charging process within one period. The indices are calculated as:

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$$V_{\mathrm{dc,avg}} = \frac{1}{T_w} \int_{t_0}^{t_0+T_w} v_{\mathrm{dc}}(t)\, dt \tag{5}$$

$$K_r = \frac{\sqrt{\frac{1}{T_w} \int_{t_0}^{t_0+T_w} \left[v_{\mathrm{dc}}(t) - V_{\mathrm{dc,avg}}\right]^2 \mathrm{d}t}}{V_{\mathrm{dc,avg}}} \tag{6}$$

$$I_{D,\mathrm{pk}} = \max_{t \in T_w} i_D(t) \tag{7}$$

$$I_{D,\mathrm{rms}} = \sqrt{\frac{1}{T_w} \int_{t_0}^{t_0+T_w} i_D^2(t)\, \mathrm{d}t} \tag{8}$$

$$\theta = \frac{T_{\mathrm{on}}}{T} \times 180^\circ \tag{9}$$

where $V_{dc,avg}$ is the average DC voltage over the steady-state window, $v_{dc}(t)$ is the DC output voltage, $V_{r,ac,rms}$ is the RMS value of the AC component of the output voltage, K_r is the ripple factor, $I_{D,pk}$ is the peak value of the reported diode charging current, $I_{D,rms}$ is its RMS value, θ is the conduction angle per charging pulse, and T is the line-frequency period. $T_{on,total}$ denotes the total effective conduction duration within the last line-frequency period. Because the full-bridge rectifier produces two charging pulses in one line-frequency period, the expression in (9) converts the total conduction duration into the conduction angle of a single charging pulse. t_a and t_b denote the start and end times of the steady-state statistical window, respectively.

The steady-state window is taken as the last four line-frequency periods. The conduction angle is calculated from the total effective conduction duration in the last line-frequency period and then converted to a single charging pulse. The conduction threshold is defined as the larger value between 0.0001 A and 0.2% of the peak current in the current period, reducing the influence of numerical noise on conduction-time estimation.

3. Simulation results and analysis

3.1. Steady-state waveforms and pulsed-charging features

A representative operating point is first examined to verify that the model captures the typical steady-state behavior of a capacitor-input rectifier. The selected case is C = 2200 μF and R_L = 50 Ω. In this case, both the voltage ripple and the current pulse are sufficiently visible, which makes it suitable for observing the correspondence between capacitor charge-discharge behavior and diode conduction.

Under this operating point, the DC-side voltage stays near a relatively high average level and shows a periodic slow decay followed by a short recovery. When the rectified voltage exceeds the capacitor voltage plus the diode conduction drops, the capacitor is recharged quickly; when the rectified voltage falls, the diodes turn off and the load is supplied by capacitor discharge. Fig. 2

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presents the steady-state AC input voltage and DC output voltage. Compared with an unfiltered full-wave rectified voltage, the trough of the output voltage is clearly lifted, and the low-frequency pulsation is reduced.

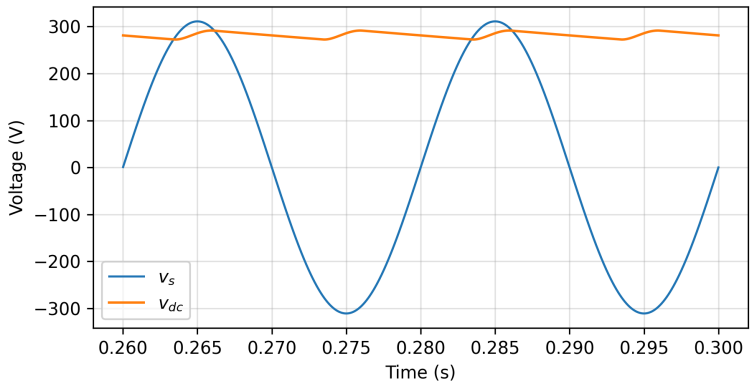

Figure 2. AC input voltage and DC output voltage under the representative case

The reported diode charging current under the same operating point reveals the other side of the filtering process. Because the capacitor voltage remains high during the non-conduction interval, the diodes conduct again only when the rectified voltage approaches the next peak. The narrow pulses in Fig. 3 show that capacitor replenishment is not distributed over the full period, but concentrated in a short time window. The later observations of increased peak current and reduced conduction angle can therefore be traced back to this pulsed-charging mechanism.

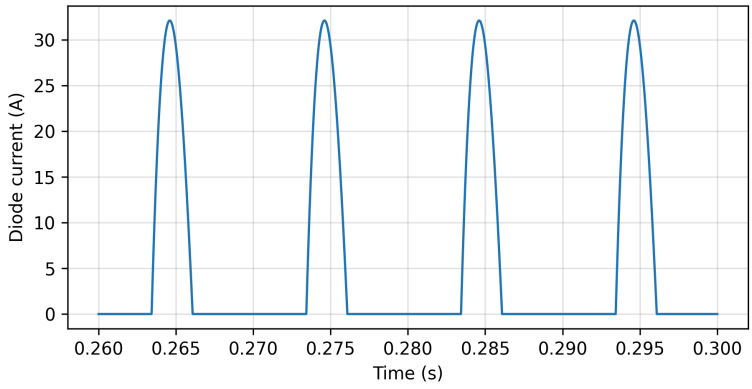

Figure 3. Diode charging-current pulses under the representative case

3.2. Effect of filter capacitance on DC output quality

The full parameter scan shows first that the filter capacitance changes the DC output quality, and that the extent of this improvement depends on the load level. Table 2 lists the steady-state indices for the fifteen capacitance-load combinations. For R_L = 50 Ω, increasing the capacitance from 220 μF to 4700 μF raises the average DC voltage from 241.84 V to 283.00 V, an increase of 17.02%, and reduces the ripple factor from 0.1751 to 0.0098, a reduction of 94.40%. The larger capacitor reduces the voltage drop caused by load discharge and keeps the DC output closer to the rectified peak.

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Table 2. Steady-state performance indices under different capacitance and load conditions

R_L / Ω	C / μF	Average DC voltage / V	Ripple factor	Peak current / A	RMS current / A	Conduction angle / °
20	220	207.92	0.3185	25.36	14.60	108.73
20	470	230.47	0.1940	39.47	18.73	83.19
20	1000	250.70	0.1017	50.72	22.31	68.61
20	2200	260.43	0.0477	55.45	23.89	63.61
20	4700	262.97	0.0225	56.62	24.31	62.68
50	220	241.84	0.1751	19.17	8.36	74.33
50	470	264.46	0.0926	26.67	10.41	57.19
50	1000	277.45	0.0455	30.81	11.59	49.41
50	2200	281.96	0.0209	32.13	11.98	47.32
50	4700	283.00	0.0098	32.42	12.08	47.03
100	220	265.63	0.0998	14.61	5.37	54.73
100	470	282.24	0.0500	18.60	6.37	43.20
100	1000	289.71	0.0240	20.33	6.82	38.76
100	2200	291.93	0.0110	20.81	6.94	37.74
100	4700	292.41	0.0052	20.91	6.97	37.58

Fig. 4 shows the ripple factor as a function of filter capacitance under different load conditions. All three curves decrease as the capacitance increases, but the slope is not constant. The improvement is most pronounced when the capacitance increases from 220 μF to 1000 μF; beyond 2200 μF and 4700 μF, the ripple continues to decrease, but the marginal benefit weakens. Load level changes the magnitude of this trend. Under the 20 Ω heavy-load condition, the capacitor discharges faster during the non-conduction interval, so the ripple factor is consistently higher than that under the 100 Ω light-load condition. Under light load, less charge is consumed within each period, and the capacitor voltage is easier to maintain. Thus, the filtering effect of a given capacitance must be interpreted together with the load condition.

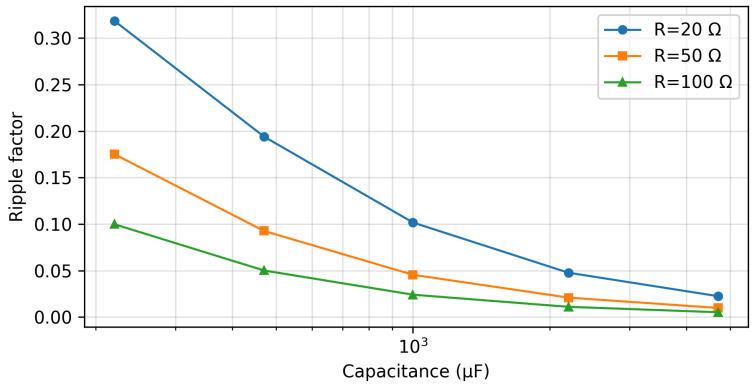

Figure 4. Ripple factor versus filter capacitance under different load conditions

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3.3. Coupled variation of current stress and conduction angle

Considering the improvement in ripple factor alone does not fully reflect the impact of large-capacitance filtering on the current stress of rectifier devices. Table 2 and Figs. 5 and 6 show that, as ripple decreases, the reported diode charging-current peak and RMS value generally increase. For R_L = 50 Ω, increasing the capacitance from 220 μF to 4700 μF raises the peak current from 19.17 A to 32.42 A, an increase of about 69.1%, and raises the RMS current from 8.36 A to 12.08 A, an increase of about 44.5%. Under the 20 Ω heavy-load condition, the peak current rises from 25.36 A to 56.62 A, an increase of about 123.3%. Therefore, heavier loading makes the current-stress amplification caused by capacitive filtering more pronounced.

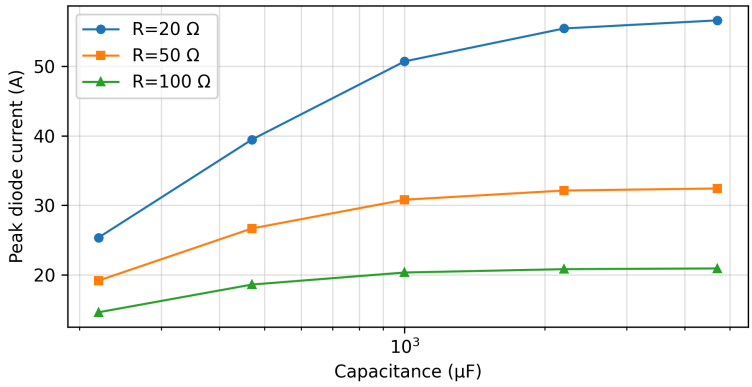

Figure 5. Peak diode charging current versus filter capacitance under different load conditions

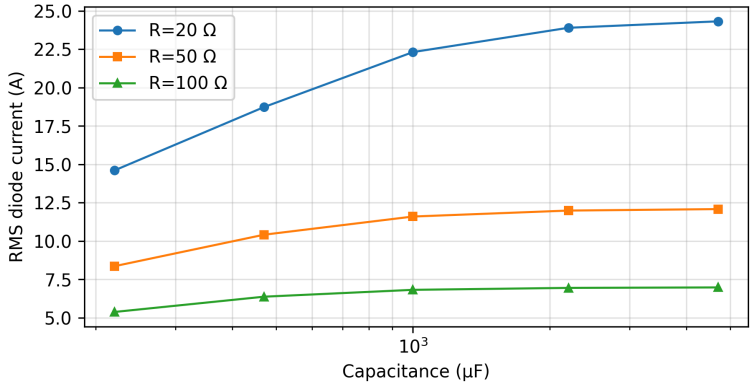

Figure 6. RMS diode charging current versus filter capacitance under different load conditions

The conduction angle provides the time-scale explanation for the increase in peak current. Fig. 7 shows that the conduction angle per charging pulse decreases as the filter capacitance increases. For R_L = 50 Ω, the conduction angle decreases from 74.33° to 47.03°; for R_L = 20 Ω, it decreases from 108.73° to 62.68°. The shorter conduction interval has to replenish the energy consumed by the load during the period, so the charging process must occur with a higher instantaneous current. The increase in peak current is therefore not a numerical coincidence; it follows from the combined effect of higher capacitor-voltage retention, delayed diode conduction, and compressed energy replenishment.

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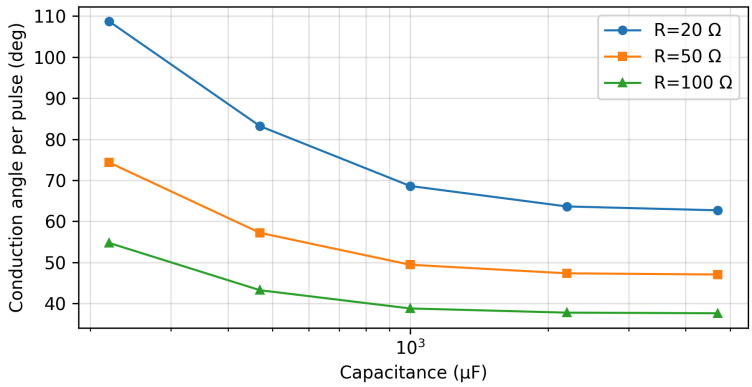

Figure 7. Conduction angle per charging pulse versus filter capacitance under different load conditions

Peak current and RMS current correspond to different device constraints. Peak current is mainly associated with instantaneous current impact and surge-current margin, whereas RMS current is more closely related to conduction loss and thermal design. In a capacitor-input rectifier, both indices usually increase with capacitance, but not at exactly the same rate. Device selection should therefore not rely on only one of them. Treating the conduction angle as an intermediate variable between output ripple and current stress helps explain how capacitance changes redistribute the waveform in time.

3.4. Integrated trade-off between ripple suppression and current stress

Taken together, the results show that capacitive filtering changes the time distribution of energy replenishment: the more stable the DC voltage is, the more the charging process is concentrated near the peak of the rectified voltage. To evaluate filtering benefit and device penalty in the same view, the ripple factor and diode charging-current peak are plotted in one coordinate frame, as shown in Fig. 8. All three load conditions exhibit the same trend: lower ripple is associated with higher peak current. Compared with the ripple curve alone, this trade-off curve better represents the practical design constraint because the filter capacitor affects output-voltage quality, rectifier current margin, thermal design difficulty, and input-side shock characteristics at the same time.

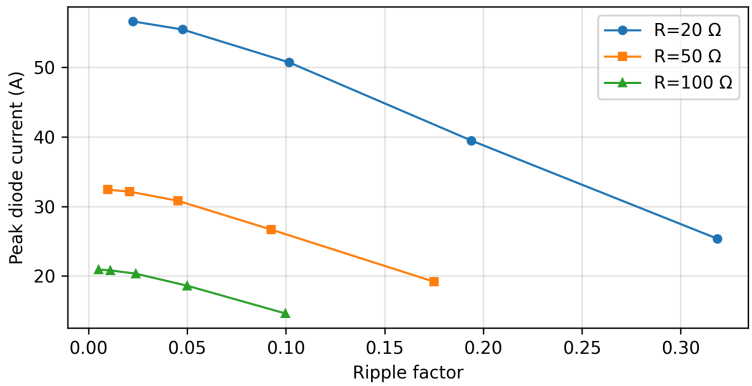

Figure 8. Trade-off between ripple factor and diode charging-current peak

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The marginal changes further show that increasing capacitance does not always produce proportional benefit. For R_L = 50 Ω, when the capacitance increases from 2200 μF to 4700 μF, the ripple factor decreases from 0.0209 to 0.0098, a relative reduction of about 53.1%; the peak current, however, increases only from 32.13 A to 32.42 A, about 0.9%, and the conduction angle changes only from 47.32° to 47.03°. In this parameter region, the source-side equivalent series resistance has already imposed a clear limitation on the charging current. Further capacitance increase mainly improves ripple, while its additional effect on steady-state peak current becomes weak. By contrast, in the 220 μF-1000 μF range, both ripple reduction and peak-current increase are significant, and the design trade-off is more sensitive.

Capacitance selection should therefore not be reduced to a simple rule that a larger capacitor is either always better or always more risky. For low-cost auxiliary supplies with relaxed ripple requirements, the smaller capacitor that satisfies the ripple target may be preferred to reduce rectifier current margin and volume cost. For loads or control loops sensitive to DC-link fluctuation, a larger capacitor may be required, but the rated diode charging-current peak, RMS current, heat dissipation, and inrush-limiting measures should be checked at the same time. Under heavy load, the capacitor discharges faster and the need for short-time energy replenishment is stronger, so device margins should not be estimated from light-load results alone.

4. Conclusion

This paper studied the trade-off between ripple suppression and device current stress in a single-phase full-bridge rectifier with capacitive filtering. A continuous-time simulation procedure including diode forward voltage drop and equivalent series resistance was constructed, and fifteen cases formed by five capacitance values and three load resistances were scanned. The results show that a larger filter capacitance increases the average DC voltage and reduces the ripple factor, but it also reduces the diode conduction angle and concentrates the charging current into a shorter time window. Thus, the effect of capacitive filtering appears not only in output-voltage smoothness, but also in charging-time distribution and rectifier current stress.

For R_L = 50 Ω, increasing the capacitance from 220 μF to 4700 μF reduces the ripple factor by 94.40% and increases the average DC voltage by 17.02%. At the same time, the diode charging-current peak increases by about 69.1%, the RMS current increases by about 44.5%, and the conduction angle per charging pulse decreases by 36.72%. Under the 20 Ω heavy-load condition, the peak current reaches 56.62 A, indicating that heavier loading further amplifies the current-stress penalty of large capacitive filtering. The mechanism is that a larger capacitor maintains a higher capacitor voltage, shifts diode conduction toward the peak of the rectified voltage, and compresses energy replenishment into a shorter time interval.

The ripple-factor versus peak-current curve shows that this type of rectifier-filter system has no unconstrained single optimum capacitance. Practical selection should consider the target ripple, load level, rectifier peak-current and RMS-current margins, thermal conditions, and system cost. For low-cost auxiliary supplies with relaxed ripple requirements, a smaller capacitor that satisfies the ripple target may be sufficient. For applications sensitive to DC-link fluctuation, a larger capacitor may be unavoidable, but soft-start circuits, NTC thermistors, series current-limiting resistors, or front-end PFC structures should be evaluated at the same time. Since the present model focuses on steady-state operation, future work can further include capacitor ESR/ESL, source-side inductance, temperature coupling, and start-up inrush processes to build a more complete device-selection and protection-design method.

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