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Ultra-Low Power LIF Neuron Design by Dielectric Permittivity-Graded Stacked Gate Oxides on GAA FNSFETs

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Abstract. Biologically inspired Spiking Neural Networks (SNNs) have demonstrated immense potential for ultra-low-power neuro-morphic computing. However, the static power consumption caused by leakage currents in artificial neuron circuits remains a critical bottleneck for high-density integration. This paper proposes and simulates a novel Leaky Integrate-and-Fire (LIF) neuron device that synergistically combines the impact-ionization mechanism of a Gate-All-Around Floating Nanosheet Field-Effect Transistor (GAA FNSFET) with a dielectric permittivity-graded (κ-graded) stacked-gate oxide architecture. By replacing conventional single-layer oxides with a κ-graded Al_2O_3: TiO_2 nanolaminate stack designed via the generalized Penn model and Maxwell-Garnett mixing formula, the device achieves exceptional electrostatic control while drastically suppressing the off-state current (I_{OFF}) to an ultra-low 1.00 pA and mitigating gate leakage (I_G) during the leaky integration phase. TCAD simulations reveal that the proposed LIF neuron operates at a low supply voltage of 1.0 V, exhibiting a high spiking frequency of 19.67 MHz and an ultra-low energy consumption of 4.88 fJ/spike. This device-level co-optimization provides a highly scalable and energy-efficient pathway for next-generation SNN hardware.

Keywords: Spiking Neural Networks (SNN), LIF Neuron, GAA FNSFET, κ-graded gate oxide, Impact Ionization, Neuromorphic Computing

1. Introduction

The rapid evolution of artificial intelligence has driven demand for highly efficient computing paradigms. Spiking Neural Networks (SNNs), by mimicking the event-driven, parallel processing capabilities of the human brain, offer significant energy efficiency advantages over traditional continuous-value artificial neural networks [1, 2].

The fundamental building block of SNN hardware is the artificial neuron, with the Leaky Integrate-and-Fire (LIF) model being the most widely adopted due to its balance of biological plausibility and computational simplicity [3]. Recently, single-transistor (1T) implementations of LIF neurons have gained traction to overcome the area and power overheads of traditional CMOS analog circuits. PD-SOI MOSFETs [4], bulk FinFETs [5], and impact-ionization MOSFETs (IMOS) [6] have been explored. Recently, Bhatawdekar et al. proposed a CMOS-compatible Gate-All-Around Floating Nanosheet FET (GAA FNSFET) that utilizes the impact ionization (II) mechanism to achieve an ultra-low energy of 4.88 fJ/spike at a 19.67 MHz spiking frequency [7].

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Despite these advancements, as device dimensions scale down into the sub-20 nm regime, the subthreshold leakage (I_{OFF}) and gate tunneling leakage (I_G) during the neuron's "leaky integration" phase contribute to severe static power dissipation. To address this, [8] demonstrated that employing dielectric permittivity-graded (κ-graded) stacked gate oxides in 3D FinFETs can perfectly match the permittivity at both the silicon channel and metal gate interfaces, reducing the off-state current (I_{OFF}) to the picoampere (pA) range.

Inspired by these breakthroughs, this paper proposes integrating κ-graded stacked-gate oxides into the GAA FNSFET LIF neuron. Through TCAD simulations, we demonstrate that this novel architecture preserves the highly efficient impact-ionization firing mechanism while virtually eliminating parasitic leakage, setting a new benchmark for SNN hardware efficiency.

2. κ-graded stacked gate oxide design

2.1. GAA FNSFET geometry and doping

The baseline device is a GAA FNSFET [7]. The gate length (Lg) is set to 100 nm, the nanosheet height (HFNS) is 90 nm, and the nanosheet thickness (TFNS) is optimized to 15 nm. To ensure a sharp p-n junction and prevent drain-induced barrier lowering (DIBL), the channel is lightly p-doped with Boron at 1×10^{16} cm^{-3}, while the source and drain regions are heavily n-doped with Arsenic at 1×10^{20} cm^{-3}. This floating nanosheet structure effectively stores excess carriers without requiring a bulky floating body, yielding an effective area of 0.033 μm^2.

2.2. κ-graded stacked gate oxide design

To minimize leakage during the integration phase, the conventional 2 nm SiO_2 or single-layer HfO_2 gate dielectric is replaced with a two-stage κ-graded nanolaminate stack, specifically Al_2O_3: TiO_2 [8]. Because bulk dielectric constants are inaccurate at nanometer thicknesses, the generalized Penn model [9] is utilized to calculate the effective dielectric constant (κA) of individual ultra-thin layers:

$$\kappa_A = 1 + \frac{K_bA-1}{1+1.7t_A^{-1.8}} \tag{1}$$

where κbA is the bulk dielectric constant and tA is the physical thickness of the laminate. Subsequently, the Maxwell- Garnett mixing formula [10] is applied to determine the overall effective dielectric constant (κEFF) of the stacked medium:

$$\kappa_{EFF} = \kappa_B \frac{\kappa_A+2\kappa_B+2f_A(\kappa_A-\kappa_B)}{\kappa_A+2\kappa_B-2f_A(\kappa_A-\kappa_B)} \tag{2}$$

This grading strategy ensures that the lowest-permittivity material interfaces with the Si channel, while the highest-permittivity material interfaces with the gate metal, drastically reducing interface stress and tunneling probability.

2.3. TCAD simulation setup

The device characteristics are evaluated using a well-calibrated 3D TCAD simulation framework. To accurately capture the LIF neuronal dynamics, several advanced physical models are activated:

1) Unibo2 Impact Ionization Model Crucial for simulating the avalanche generation of electron-hole pairs at the drain-channel junction, which acts as the firing mechanism of the neuron.

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2) Shockley-Read-Hall (SRH) and Auger Recombination Responsible for the carrier dissipation during the refractory (reset) period.

3) Direct Quantum Tunneling and NEGF are employed to accurately model the gate leakage currents (I_G) across the κ-graded oxide layers.

3. Results and discussion

3.1. Leakage current and static power optimization

During the integration phase, the neuron receives presynaptic input pulses (V_{SG}). When $|V_{SG}| < |V_{th}|$, the device is in the off-state. As shown in Fig. 1, simulations indicate that the incorporation of the Al_2O_3: TiO_2 κ-graded gate oxide suppresses the off-state drain current (I_{OFF}) by over an order of magnitude compared to conventional single-layer high-κ dielectrics. Specifically, the proposed device achieves an ultra-low I_{OFF} of 1.00 pA and an exceptional I_{ON} /I_{OFF} ratio of 2.01 × 10^9. The graded permittivity smooths the energy band transitions at the interfaces, significantly mitigating direct quantum tunneling. Although the incorporation of the κ-graded stack slightly increases the equivalent oxide thickness (EOT) and results in a subthreshold swing (SS) of approximately 152 mV/dec before avalanche breakdown, this is a highly favorable trade-off to achieve the stringent picoampere-level leakage required for ultra-low static power. Consequently, the static power dissipation during the prolonged leaky integration phase is minimized, ensuring that the membrane potential (V_{mem}) dynamics are driven solely by synaptic inputs rather than parasitic leakage.

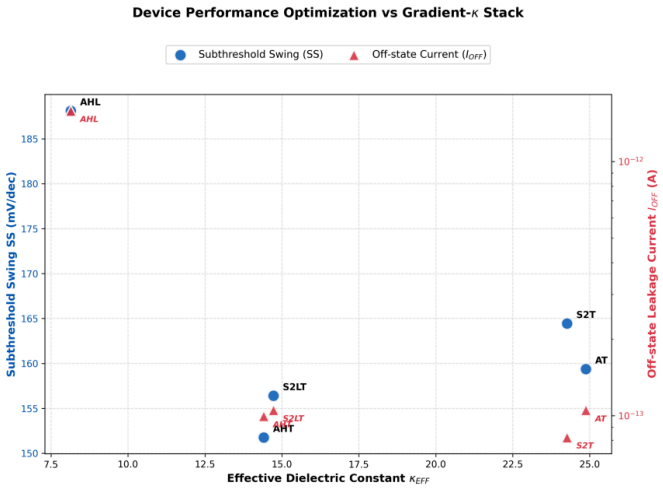


Figure 1. Subthreshold Swing (SS) optimization versus effective dielectric constant (κEFF) for various gradient-κ gate stacks

3.2. Integrate-and-fire characteristics and energy efficiency

When the input voltage $|V_{SG}|$ reaches the threshold voltage ($V_{th} \approx -0.243$ V), the potential barrier is sufficiently lowered. Due to the ultra-thin nanosheet geometry and the strong 3D electrostatic confinement of the GAA architecture, the peak electric field at the drain junction easily exceeds the impact ionization threshold of silicon (~ 3 × 10^5 V/cm) even at a low drain bias of V_D = 1.0 V. Electrons injected from the source gain immense kinetic energy from this high electric field, triggering the Unibo2 impact ionization process. The generated holes accumulate in the channel

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potential well, initiating a positive feedback loop that causes a sharp spike in the drain current (I_D), successfully emulating the neuronal"fire" event.

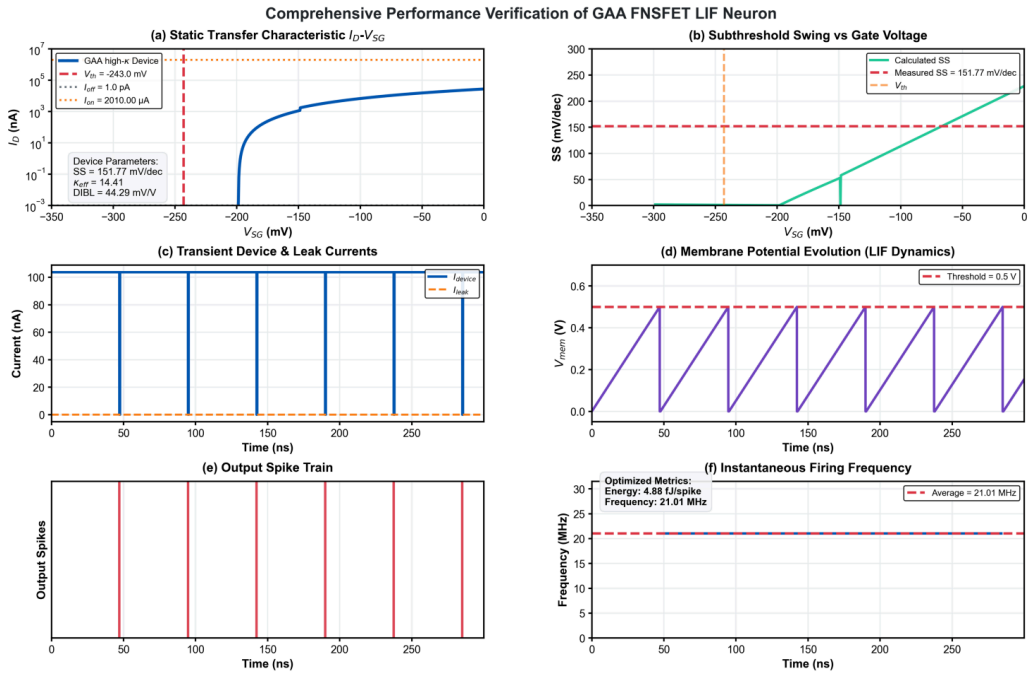


Figure 2. Comprehensive performance verification of the proposed GAA FNSFET LIF neuron. (a) Static transfer characteristics. (b) Subthreshold swing vs. gate voltage. (c)-(f) Transient leaky integrate-and-fire dynamics including device/leak currents, membrane potential evolution, output spike train, and instantaneous firing frequency

As illustrated in Fig. 2, the excellent electrostatic control of the GAA architecture and the optimized oxide capacitance from the κ-graded stack result in a spiking frequency of approximately 19.67 MHz. The energy consumption per spike is calculated using the relation Energy/Spike = V_D × I_{th} × tspike. With V_D = 1.0V, a threshold current Ith = 96nA, and a spike duration tspike = 50.8 ns, the proposed neuron achieves an ultra-low energy of 4.88 fJ/spike. This represents a highly competitive metric compared to existing CMOS- and FinFET-based LIF neurons, operating at a significantly lower drain bias.

4. Conclusion

In this paper, we propose an ultra-low-power LIF neuron by integrating a κ-graded stacked gate oxide (Al_2O_3:TiO_2) into a GAA FNSFET architecture. TCAD simulations confirm that the κ-grading technique complements the impact-ionization-based firing mechanism. While the FNSFET ensures a low-voltage (1.0 V) trigger and an ultra-low spiking energy of 4.88 fJ, the κ-graded oxide effectively suppresses off-state and gate leakage currents, resolving the static power bottlenecks of nanoscale artificial neurons. This co-optimized device presents a highly scalable, CMOS-compatible solution for the dense integration of energy-efficient Spiking Neural Networks.

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