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Discussions and Recommendations Based on the Existing Structure of the LDO

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Abstract. With the development and popularization of various electronic products, the demand for small-scale integrated power chips is gradually increasing, especially in applications such as mobile phones, computers, and spacecraft. Low dropout linear voltage regulator devices (LDOs) are widely used as excellent characteristics such as high integration and low output ripple. At present, the research on LDO is mainly for the optimization and compromise of various parameters, such as module area, power rejection ratio, transient response, static power consumption, etc. This article analyzes and discusses LDO structures with no off-chip capacitance, high power supply rejection ratio, and high transient response. The compensation scheme and design innovation used are summarized. To discuss high-performance LDO schemes by referring to existing LDO structures.

Keywords: off-chip capacitor, high transient response, high PSRR

1. Introduction

At present, the mainstream DCDC step-down is usually composed of a switching power supply, a forward and a backlash power supply, an LDO, and other power supplies. Compared with other DCDC power supply solutions with high ripple, large volume, and high output capacity, LDO has excellent characteristics such as small size and low output noise. As the current mainstream low-voltage power supply chip, it is often used as a back-stage power supply for DCDC to power high-precision circuits, such as mobile phone computer chips, because its input voltage is the power supply characteristic, which is generally composed of a reference voltage reference source and an amplifier feedback loop. At present, LDO mainly has off-chip capacitance-free research directions, high transient response and high supply noise.

Compared with off-chip capacitive LDOs, since there are no external capacitors to provide output filtering, the existence of feedback will cause the sudden change of load current to have a certain impact on the input of the op amp, which will reduce the overall response of the circuit

The main research hotspots of LDO include LDO chips with or without out-of-chip load capacitors, LDO chips with high supply noise suppression, novel frequency compensation schemes, and optimization of LDO transient response [1]. For off-chip load capacitors, due to the small size of the LDO itself, the redundant off-chip capacitors will increase the overall area of the power module. However, capacitors also have the effect of suppressing overshoot voltages and stabilizing the LDO internal loop [1]. Therefore, LDO without external load capacitor, which compensates for LDO

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performance (such as response and bandwidth) by auxiliary modules, has become one of the research hotspots. At the same time, due to RF, phase-locked loops, and other module applications with high power supply requirements, LDO needs to have a high power supply ripple rejection ratio in different frequency domains [2].

This review will summarize and analyze the innovations and characteristics of these three new LDO studies. It points out the improvement effect brought by each LDO innovation point and the corresponding improvement requirements of LDO in the future.

2. Out-of-chip capacitor-less LDO

Regarding the auxiliary circuit part, due to the special requirement of no off-chip capacitor, the role of traditional capacitor loop compensation needs to be reflected through other modules.

Xie Leijing et al. first used a push-pull structure of a double differential loop to separate the original poles and generate intermediate compensation poles to improve the phase margin and increase the response capability. At the same time, considering the work efficiency at low load, a cross-coupled source-follower adaptive bias circuit is introduced, which can simply amplify and regulate the transistor current in the differentiator through a galvanoscope to realize the rapid charging and discharging of gate capacitors, and ultimately improve the response speed [3]. The system reduces the area of on-chip capacitors through the dual Weifen control structure, and effectively improves the phase margin and transient response of LDO under the condition of ensuring ground static power consumption, and has the characteristics of superior transient performance, low power peak amplitude and short recovery time compared with traditional LDO.

Óscar Pereira-Rial proposed a super-source adherent (SSF) structure that introduces an error amplifier input and uses it to achieve adaptive bias. This method dynamically adjusts the bias current by detecting the voltage difference at the input of the error amplifier [4]. When the load current changes, the bias current increases with the input difference, thereby improving the transconductivity and driving capability of the amplifier, speeding up the charging and discharging process of the power pipe gate, and improving the transient response performance of the circuit. At the same time, maintaining a low bias current under steady-state conditions helps reduce power consumption.

SHAO-KU KAO et al. directly use the error amplifier output signal to construct a feedforward path, and adjust the loop frequency response through this path, so as to improve the stability of the system. Unlike traditional LDOs, they introduce negative feedback or feedforward signals at the input of the error amplifier [5]. The feedforward action point is set at the output of the amplifier, which can shorten the signal transmission path, improve the transient response speed, and facilitate the introduction of a compensation zero point to enhance the loop stability.

In this method, an overshoot suppression circuit is introduced at the output of the error amplifier to improve the transient response performance without out-of-chip capacitance. When the output voltage is overshoot, the power pipe gate voltage is adjusted through the negative feedback path to reduce the drive current, thereby suppressing the output fluctuation and speeding up the recovery process, thereby improving the transient response speed of the circuit [6].

This method introduces a low-power output voltage detector as an auxiliary module. The detector is based on an RC high-pass filter to detect rapid changes in output voltage. When the load current changes significantly, the detector senses transient fluctuations and activates an additional control pathway. This path has the characteristics of high bandwidth and low gain, and can quickly adjust the source-accompanied power tube, thereby improving the transient response performance of the circuit [7].

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Marouf Khan et al. introduced a PMOS and NMOS cascade structure between the error amplifier and the power tube. Among them, PMOS is used as a power tube to reduce the voltage drop voltage, which is suitable for low voltage margin applications. At the same time, by cascading NMOS devices on the PMOS, the power supply noise is isolated, thereby improving the power rejection ratio (PSRR). In addition, an RC low-pass filter is introduced at the NMOS gate to suppress the coupling of power supply ripple to gate, further improving PSRR performance [8]. This structure effectively enhances the circuit's ability to resist power interference through a multi-stage suppression mechanism.

3. High power supply rejection ratio LDO

Jung Sik Kim et al. proposed the intrinsic gain tracking ripple cancellation (IGTRC) technique, which works in tandem with the main control loop by constructing an auxiliary path composed of an intrinsic gain tracking module, a buffer and an output capacitor. The method uses a summing amplifier to superimpose the output signal of the error amplifier with the ripple cancellation signal generated by IGTRC, so as to achieve the cancellation of the power supply ripple at the output end. Unlike traditional multi-stage op-amp-based feedforward techniques, this method eliminates the need for additional auxiliary amplifiers or complex reference circuits, reducing circuit complexity and power overhead. Therefore, this technology has the advantages of small area and simple implementation. From a mechanistic point of view, the proposed method enhances the effective output capability of the error amplifier through signal superposition, thereby improving the power supply rejection ratio, which provides a new implementation idea for LDO high PSRR design [9].

Huang Jingwei's main method is to improve the power supply suppression ratio of LDO from three aspects. In the reference source design, the feedback voltage is directly introduced into the reference circuit, so as to avoid the noise interference caused by the traditional feedback resistor. At the same time, a current-mode reference structure is adopted, and the reference voltage is generated through the internal reference current source and the external resistor, and the capacitors are connected in parallel at both ends of the external resistor to further suppress the resistance noise. In addition, BJT is used for signal amplification at the input stage of the error amplifier, and compensation is introduced to improve system stability and high-frequency performance [2]. The innovation of the reference source structure in this literature is that the reference voltage is generated by an external resistor and an on-chip reference current source, rather than completely relying on the on-chip voltage reference. Compared with the traditional LDO, the structure directly uses the feedback voltage as the input of the op amp and feeds its output to the post-amp buffer, so that the system error is mainly determined by the common mode error of the post-amp, which effectively reduces the error source and improves the power supply suppression ability.

On the basis of fully considering that the LDO itself has a certain suppression ability for input ripple, Wu Jiaqi et al. used a multi-stage cascade structure to further improve the overall power supply suppression ratio of the system. Specifically, by constructing a three-stage LDO cascade architecture, the step-by-step regulation and filtering of the input voltage, reference voltage and output voltage are realized. Firstly, the pre-stage LDO is introduced at the input end to pre-regulate the input voltage to generate a more stable secondary power supply and reduce the amplitude of the input ripple from the source. Secondly, the second stage LDO is introduced at the reference end to regulate the reference voltage, and combined with low-pass filtering and voltage following structure, the noise and low-frequency ripple in the reference path are effectively suppressed, so as to significantly improve the low-frequency PSRR performance of the system. Finally, the output regulation is completed through the third-stage LDO, and the system stability and mid- and high-

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frequency suppression capabilities are optimized by combining the compensation and feedforward structure [10]. Through the synergy of the above multi-level regulation and filtering, the hierarchical suppression of ripple in different frequency bands is realized, and the power supply rejection ratio of the overall LDO is improved.

4. Fast transient response LDO

Without the need for off-chip capacitors, Lei Wang et al. adopted a double-ring LDO design based on a hierarchical couplet structure to improve system performance. Among them, the inner ring acts on the power tube path and realizes fast local negative feedback by sensing the change of output voltage and directly adjusting the gate voltage of the power tube, thereby improving the loop bandwidth and speeding up the transient response speed. The outer ring acts on the error amplifier path, which improves the DC gain and steady-state accuracy of the system by generating a stable reference voltage and introducing high gain regulation, thereby enhancing the power supply rejection capability. Through the synergy of the inner and outer loops, fast response and high PSRR performance are achieved without the need for large-area out-of-chip capacitors [11].

This method adopts a transient enhancement circuit based on capacitive coupling to improve the response speed of LDO when the load is abrupt. The rapid change of output voltage is detected through the Qualcomm network composed of capacitors and resistors, and the auxiliary path is triggered when the load is switched from light load to heavy load, providing a fast discharge path for the power tube gate, thereby speeding up the power tube conduction speed, reducing the output voltage down rush and improving the transient response performance. Unlike traditional methods that rely on large output capacitors for energy storage, this method achieves performance improvement without the need for off-chip large capacitors by introducing a fast dynamic path, making it more suitable for on-chip system design [12].

5. Suggestions for future research

In summary, most of the improvements of existing LDOs focus on transient response, output noise, and on-chip and off-chip capacitance. However, it can be found that most of the research ideas of new LDOs are often to introduce a certain improvement structure and then further compensate or optimize the new problems brought about by it, which still belongs to the category of "local improvement" as a whole. Therefore, it is necessary to explore a more versatile LDO structure in subsequent research to enable it to have good performance in different application scenarios, which still requires further innovation and improvement from the circuit structure level. Judging from the current research situation, the main factor limiting LDO performance is still focused on the trade-off between bandwidth and transient response. While performance can be improved to some extent by introducing larger capacitance or reducing circuit noise, these approaches often present problems in terms of area, power consumption, or integration. Therefore, how to achieve synergistic improvement of bandwidth and transient performance through design concept optimization without relying on additional capacitance and increasing chip area to adopt more complex structures still needs to be studied in depth.

6. Conclusion

For LDO without out-of-chip capacitor, the auxiliary circuit is usually improved by the auxiliary circuit part, and the compensation auxiliary circuit is designed to achieve this purpose by using pole

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separation compensation as the goal. For LDOs with high power supply rejection ratios, they are usually directly oriented towards reducing input/output noise or improving the structure. The study of transient high-response LDO itself is based on these external defects. In short, the current stage of LDO research is closely related to its output characteristics and working environment and specific requirements, but the hardware circuit of LDO is relatively fixed, consisting of only four parts: error amplifier, reference source, power tube and auxiliary module, but it is still very meaningful to produce a specific working situation and high-performance LDO through the study of different materials and parameters.

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