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Research Progress on Low-Power and Broad-Spectrum Neuromorphic Synaptic Transistors

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Abstract. To overcome the high power consumption limitation of the traditional von Neumann architecture where memory and computation are separated, neural morphological devices inspired by the memory and information processing mechanisms of the human brain have received considerable attention in recent years. These devices achieve efficient parallel computing and low energy consumption by simulating the behavior of biological synapses. This article reviews the latest research progress of low-power, wide-bandwidth neural morphological devices based on transistor structure design. Firstly, the basic functions of biological synapses and neurons are introduced, providing a theoretical basis for device design. Subsequently, the latest research progress of three main types of synaptic transistors, including ferroelectric gate transistors, perovskite transistors, and electrolyte gate transistors, is discussed in detail, along with their working mechanisms, advantages, and limitations. A horizontal comparison is also conducted. Finally, the current challenges are summarized and the future development directions of neural morphological synaptic transistors are envisioned.

Keywords: Synapse, low power consumption, wide bandwidth

1. Introduction

With the rapid development of artificial intelligence, big data, and the Internet of Things, traditional computing systems are increasingly constrained by limitations in efficiency and energy consumption. Most existing systems are based on the von Neumann architecture, which separates memory and processing units. This separation requires frequent data transfer between storage and computation, resulting in limited processing speed and increased energy consumption [1]. Neuromorphic computing, inspired by the information processing mechanisms of the human brain, offers a promising approach to overcoming these challenges. By emulating the interactions between neurons and synapses, neuromorphic systems enable efficient and low-power information processing. Current implementations based on CMOS technology can realize artificial neurons and synapses [1]; however, they often require a large number of transistors, leading to complex architectures and high energy consumption. For instance, the TrueNorth chip integrates billions of transistors to simulate large-scale neural networks, yet further implementation of synaptic plasticity would demand even greater hardware resources [2]. To address these limitations, emerging neuromorphic transistors that integrate memory and computation have attracted increasing attention.

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These devices significantly reduce circuit complexity and energy consumption while enabling efficient signal processing. This review focuses on recent advances in low-power, wide-spectrum neuromorphic devices. It summarizes the working principles of typical neuromorphic transistors and analyzes their performance in terms of energy efficiency and response bandwidth, providing insights into future development directions.

2. Biological synaptic and neuronal functions

The nervous system processes information through electrical and chemical signaling between neurons, with synapses as key structures for transmission (Figure 1). A neuron consists of a cell body, dendrites, an axon, and a presynaptic terminal. Dendrites receive inputs, while the cell body integrates them. When the membrane potential reaches a threshold, an action potential is generated at the axon initial segment and propagates along the axon. When reaching the presynaptic terminal, the action potential triggers neurotransmitter release into the synaptic cleft. These molecules diffuse across and bind to receptors on the postsynaptic neuron, modulating its membrane potential. Excitatory inputs generate excitatory postsynaptic currents (EPSCs), bringing the neuron closer to firing, whereas inhibitory inputs generate inhibitory postsynaptic currents (IPSC), suppressing activation [1]. In neuromorphic electronics, such synaptic functions are emulated by devices. In transistor-based systems, the gate represents presynaptic input, while the source-drain channel corresponds to postsynaptic response. Through material and device design, these systems mimic synaptic behaviors including transmission and plasticity, providing a hardware basis for brain-inspired computing.

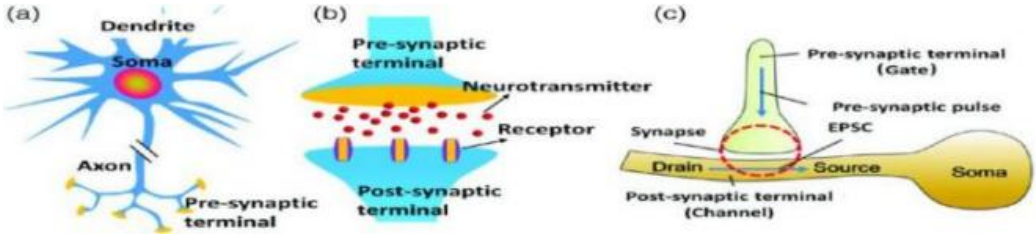


Figure 1. (a) Diagram of a neuron (b) Diagram of a synapse (c) Diagram of an artificial synapse [2]

3. Classification of mainstream neuromorphic transistors

3.1. Ferroelectric gate-type synaptic transistor

In recent years, ferroelectric gate field-effect transistors (FeFETs) have attracted significant attention due to their low power consumption and high-speed response and have been used to simulate biological synapses. Compared with traditional field-effect transistors, the key feature of field-effect transistors lies in the use of ferroelectric materials with spontaneous polarization characteristics in the gate dielectric layer, which enables non-volatile charge control through polarization reversal. Common ferroelectric material systems include traditional perovskite ferroelectric materials such as Pb(Zr, Ti)O_3 (PZT) and the recently highly regarded two-dimensional ferroelectric materials CuInP2S6. Additionally, two-dimensional material devices based on van der Waals (vdW) heterostructures, such as the WSe2/In2Se3 structure, have also been widely used to construct neuromorphic synaptic devices with photoelectric responses [3,4].

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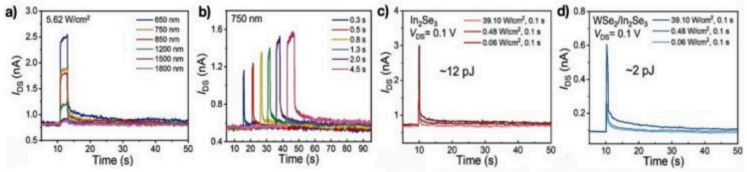


Figure 2. (a, b) PSC responses under different wavelengths and pulse durations (c, d) energyconsumption of In_2Se_3 and WSe 2/In_2Se_3 devices [3]

In terms of representative studies, Li et al. utilized the photoelectric properties of In_2Se_3 in the visible light to short infrared wavelength range to design a photosynaptic device based on the WSe_2/In_2Se_3 heterostructure. The experimental results (Figure 2) indicated that this device exhibited stable light response within the wavelength range of 650 to 1800 nanometers and could enhance the synaptic current (PSC) and delay the recovery process by adjusting the duration of the light pulse, demonstrating a transition from short-term plasticity (STP) to long-term plasticity (LTP). Additionally, due to the p-n junction structure formed by the heterostructure effectively suppressing the dark current, the PSC was reduced to approximately 10^{-11} A, significantly reducing the energy consumption of the device. Comparative experiments showed that the WSe_2/In_2Se_3 heterostructure device outperformed the In_2Se_3 transistor with lower energy consumption [3].

Furthermore, Shang et al. fabricated a three-terminal photonic synaptic transistor based on the two-dimensional ferroelectric material $CuInP_2S_6$ (CIPS) in 2024. Figure 3a shows the crystal structure of CIPS, where the hopping of Cu1 is regarded as a factor of the ferroelectric switch. As shown in the figure, the device adopts a sandwich structure, where CIPS serves as the channel layer connecting the Pt drain electrode, SiO_2 serves as the gate insulating layer, and the highly conductive silicon substrate serves as the bottom electrode under SiO_2. Under gate voltage modulation, the eccentric displacement of Cu^+ ions in CIPS induces an internal electric field, thereby regulating the generation of electrons by light being driven towards or away from the CIPS/SiO_2 interface and changing the polarization state and synaptic weight of the device, achieving the learning and memory functions similar to biological synapses and successfully simulating the photoreceptor's light adaptation behavior [4, 5]. Experimental results show that under a single light pulse (450 nm, 0.241 mW cm^{-2}, 100 ms) excitation, the electrical energy consumption of each synaptic event is approximately 0.36 pJ. After accounting for the energy losses in the electrical and optical paths, the total energy consumption is approximately 0.7 pJ.

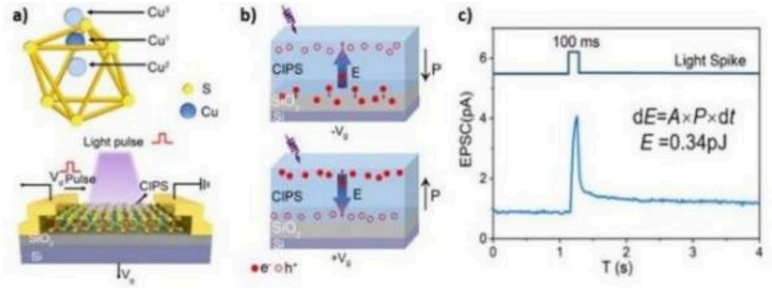


Figure 3. (a) Cu+ ion configurations and device structure (b) schematic of photogeneratedcarrierseparation under different CIPS polarization states (c) EPSC response to a single light pulse [4]

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3.2. Perovskite synaptic transistors

The solution-processed halide perovskites, due to their excellent photoelectric properties and tunable structure, are considered potential candidate materials for the next-generation neuromorphic imaging technology. Halide perovskites not only possess the advantages of inorganic semiconductors such as high absorption coefficient, tunable bandgap, and long carrier diffusion length but also have the flexibility and processability of organic materials. Moreover, these materials can simultaneously control photogenerated ions and electron charges, thereby promoting the development of complex neuromorphic devices [6,7]. Therefore, perovskite-based synaptic transistors show broad application prospects in simulating biological synaptic plasticity and photoelectric sensing functions.

In terms of representative research, Wei et al. demonstrated for the first time a bottom-gate top-contact synaptic transistor based on organic-inorganic hybrid perovskites (OHPs) and electrolyte in 2023 for simulating neural synapses. This device was fabricated by solution processing and has the advantages of a simple process, low cost, and large-area fabrication. Experimental results show that OHP materials have been used in the field of neuromorphic electronics due to their various high-quality characteristics, including absorption, bandgap, diffusion length, bipolar charge transport, and activation energy. The single synaptic event of this synaptic transistor consumes the minimum energy consumption of approximately 47 fJ, and after 2500 mechanical bending tests, its synaptic response remains at 74–86% of the initial level [8].

2025, Liu et al. used a multi-site chelating strategy to use lead-free and non-toxic methylamine triiodide (FASnI3) perovskite with a biofriendly quercetin (QR) molecule and achieved an excellent near-infrared response and photoelectric performance. As shown in Figure 4a, this device exhibits wide spectral absorption characteristics in the 400 to 900 nanometer wavelength range, and achieves efficient carrier separation through the heterojunction structure formed between the FASnI3 perovskite layer and the PEDOT: PSS layer. Due to the low exciton binding energy of perovskite materials, the electrons and holes generated after light excitation can be separated rapidly. The holes migrate to the PEDOT PSS layer, while the electrons are restricted in the perovskite layer due to the higher potential barrier, thereby forming stable photogenerated charge accumulation. As shown in Figure c, due to the long transmission distance of the holes, the device generates a slowly rising photocurrent under illumination conditions and exhibits a slowly decaying excitatory synaptic post-spike (EPSC) characteristic after the light is turned off, similar to the response process of biological synapses. In addition, the energy consumption of a single synaptic event of this device is approximately 0.24 nJ, and it can simulate the Ebbinghaus forgetting curve at the hardware level, which describes the human memory and forgetting behavior [9].

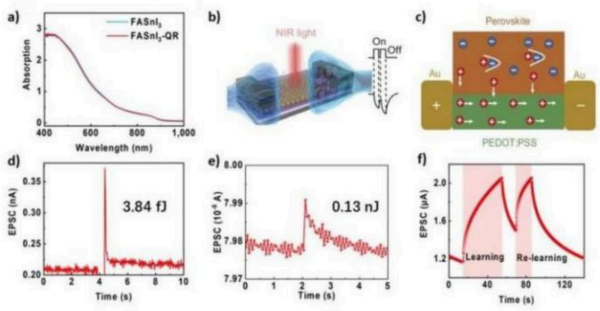


Figure 4. (a) Absorption spectra of FASnI3 and FASnI3-QR films (b) device structure (c) schematicof synaptic behavior mechanism (d, e) electrical and optical energy consumption of EPSC(f)EPSC-based simulation of memory forgetting [9]

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3.3. Electrolyte gate synapse transistor

Electrolyte gate transistors (EGTs) are a type of basic form device that regulates the conductivity of the device channel by adjusting the ions in the electrolyte dielectric layer. John et al. pointed out that the migration of ions in the electrolyte under an applied electric field is very similar to the release of neurotransmitters under an action potential [10]. In the neural morphology analogy, the gate electrode of the EGT can be regarded as the end of the nerve axon, the semiconductor channel as the postsynaptic membrane, and the channel conductance as the synaptic weight.

So far, electrolyte gate synapse transistors have made significant progress in achieving synaptic-like functions. To further simulate the application of the human visual system, Serghiou et al. proposed a neural morphology device based on an electrolyte gate-controlled organic field-effect transistor (EGOFET) in 2025. This device uses BuPTCD as the organic active layer and drop-casted honey as the gate electrolyte. The various ions in the drop-casted honey are responsible for forming an Electrical Double Layer (EDL) at the honey/perylene interface, thereby increasing IDS (EPSC) and delaying the discharge process. The formation of the EDL and the release process are similar to the charging and discharging mechanism of a capacitor, causing the device to exhibit a slow charge release process. When more charges accumulate in the channel, the relaxation time of the device becomes longer, thereby exhibiting the synaptic enhancement effect. Experimental results show that this EGOFET device requires only approximately 2.4 pJ per synaptic event on average and can operate stably under low voltage conditions (Figure 5). This characteristic provides the possibility of constructing large-scale, low-power neural morphology synapse arrays and applications. In addition, the research team also provided a different scheme from traditional technologies, combining EGOFET with machine learning training to simulate the ability of the device to mimic the light receptors in the human retina, achieving the purpose of distinguishing different light wavelengths and lighting intensities [11].

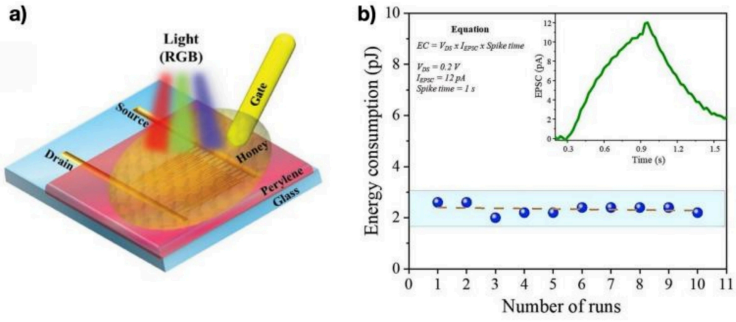


Figure 5. (a) Device structure (b) energy consumption per spike in tested 10 times [11]

4. Comparison of synaptic transistors

Table 1 compares the performance of representative synaptic transistors, highlighting the trade-offs among different material systems. Ferroelectric synaptic transistors exhibit excellent stability, fast switching speed, and strong data retention, making them suitable for high-speed and low-power neuromorphic computing. However, their operation often requires relatively high voltages to induce partial polarization switching, and challenges such as interface defects, fatigue effects, and process compatibility remain. Perovskite-based synaptic transistors offer excellent photoelectric response capabilities and tunable bandgaps, which enable integrated sensing and computing functionalities. However, most devices rely on lead-based materials, raising concerns about toxicity and limiting

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their applicability in biocompatible systems. In addition, the fabrication of environmentally friendly perovskites often involves higher costs.

Electrolyte-gated synaptic transistors are particularly effective in mimicking dendritic and synaptic behaviors, and their low-voltage operation enables ultra-low energy consumption. However, device stability, especially related to ionic materials, remains a key challenge for large-scale integration and practical applications.

Table 1. Materials and performance comparison of different types of synaptic transistors

	Channal material	Power consumption	Absorption spectrum	Synaptic/neuronal function
Ferroelectrics [3, 4]	WSe 2/In 2Se3	2pJ	650-1800nm	EPSC; PPF Short/Long-term Plasticity
	CIPS	0.36pJ	~450nm	EPSC; PPF Short/Long-term Plasticity
Perovskite [8,9]	OHPs	47fJ	400-800nm	PPF; SDDP; SFDP
	FASnI3 with QR	0.24nJ	400-900nm	EPSC;PPF; SNDP Short/Long-term Plasticity
Electrolyte gate material [11]	BuPTCD and drop-casted honey	2.4pJ	380~750nm	EPSC; PPF Short/Long-term Plasticity

5. Conclusion

Recent advances in neuromorphic computing have accelerated the development of synaptic transistors with low power consumption and wide spectral response. As computational demands continue to grow, memory-computation integrated devices have emerged as a promising hardware solution to overcome the limitations of conventional architectures, enabling improved energy efficiency and reduced training time. This review summarizes recent progress in neuromorphic devices based on ferroelectric materials, perovskites, and electrolyte-gated transistors and compares their performance in terms of energy consumption and material characteristics. These devices are capable of emulating synaptic functions under lower operating voltages, with energy consumption per synaptic event typically at the picojoule level, demonstrating great potential for building high-efficiency neuromorphic systems.

However, significant challenges remain. Device performance varies across material systems, particularly in terms of power consumption and spectral response. In addition, issues such as high preparation costs and limited scalability hinder their near-term commercialization. Furthermore, this review primarily focuses on material systems, while aspects such as device structure optimization, system-level integration, and co-design strategies are less explored. Variations in testing conditions and evaluation metrics across studies also limit the direct comparability of reported results. Future research should focus on large-scale integration of ultra-low-power neuromorphic devices, as well as the development of standardized evaluation frameworks. Such advances will facilitate their applications in areas including image recognition, intelligent robots, bio-integrated intelligent chips, and health monitoring systems.

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