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# *Core Peripherical Circuit Design for High-Capacity STT-MRAM*

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***Abstract.*** STT-MRAM has become a potential technique in System-on-Chip(SoC) application depending on low consumption, high-density, high speed and non-volatility. Parasitic resistance and capacitance in high-capacity STT-MRAM have higher requirements for high-accuracy read-and-write circuits. This paper elaborates on a sense amplifier with a high sensing margin, which can effectively improve the reading accuracy. It also reviews the adaptive self-termination circuit, which can effectively alleviate the high write power consumption and unnecessary write delay caused by the fixed write pulses in traditional write operations. Furthermore, this paper reviews the relevant circuit design schemes, including wordline driver circuits, for the problem of insufficient write drive in large-capacity arrays, which provides design references for improving the stability and reliability of the overall circuit.

***Keywords:*** STT-MRAM, SoC, sense amplifier, self-termination circuit, wordline driver circuit

## 1. Introduction

Spin-Transfer Torque Magnetic Random Access Memory (STT-MRAM) is emerging non-volatile memory technology featuring ultra-low power consumption, ultra-fast access speed and excellent compatibility with CMOS fabrication processes. It is a key candidate for next-generation memories in highly integrated and low-power system-on-chip (SoC) systems. The optimized design of core peripheral circuits is key to the practical application of high-capacity STT-MRAMs. On the one hand, sense amplifiers with high sensing margins can effectively identify weaker read signals in large-capacity arrays, thereby significantly improving the read accuracy. However, in high-capacity applications, write self-termination circuits can detect the write completion state in real time and terminate write pulses precisely, thus optimizing the speed of write operations. Focusing on the optimization of read-write performance and the suppression of IR-drop effects, this paper systematically summarizes the existing design and optimization strategies of key modules, including sense amplifiers, write self-termination circuits, and wordline driver circuits. This review provides a systematic reference for the circuit design and integration of high-capacity STT-MRAMs in SoCs.

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## 2. Key circuit design for high-capacity STT-MRAM

### 2.1. Preliminary

In a conventional 1T1MTJ STT-MRAM cell, during the read operation, the word line selects the target cell, and a small read current flows through the MTJ [1]. The sense amplifier converts the weak resistance difference of the MTJ into a detectable, digital signal. In the write operation phase, bidirectional write currents are driven by the differential voltage across the bit line and source line, which flips the magnetic state of the MTJ to complete the data writing.

### 2.2. High sensing margin sense amplifier

A research group at Nanjing University of Aeronautics and Astronautics presented a Dual-Swing-Sample-and-Couple Sense Amplifier (DSSC-SA) for STT-MRAM in 2025 IEEE TCAS II [2]. This circuit uses a data cell combined with dual reference cells and doubles the sensing margin through three-phase operation. It suppresses current fluctuations using source degeneration transistors. Simulations show that its sensing margin reaches 1.83 times that of conventional circuits, with a read yield of 99.9% at a sensing time of 2 ns. It also reduces power consumption and read disturbance, providing a highly reliable read circuit solution for STT-MRAM in deep-nanometer-scale technology.

In 2017, the Offset-Canceling Current-Sampling Sense Amplifier (OCCS-SA) was proposed by researchers from Yonsei University and Qualcomm Inc. in the IEEE Journal of Solid-State Circuits (2017) [3]. To solve the sensing margin degradation of STT-MRAM under the deep sub-micrometer process, a sense amplifier is designed to integrate offset voltage cancellation, a dual sensing margin architecture, and robust positive feedback, with a two-phase operation mode and double sensing margin switches for the ground DC current path. A 32×32 SA array was implemented based on a 65 nm CMOS process. The test results show that its sensing time is 2.4 times faster than that of the traditional scheme, the operating voltage is reduced by more than 20% with an area overhead of less than 10%, and the offset tolerance is much higher. It provides a high-sensing-margin SA design for high-capacity STT-MRAM and lays a technical foundation for optimizing deep-submicrometer memory read circuits.

Kyongsoo Kim, Taehwan Kim and Jongsun Park from Korea University did a research about a Data Cell Dynamic Reference (DCDR) sensing scheme for STT-MRAM [4]. This scheme abandons the traditional intermediate-resistance reference cell and uses a P-state data cell as the dynamic reference. It consists of a precharge module, a signal generator unit with two half-Schmitt triggers, a sample-and-hold (S&H) module, and a sensing amplifier. By dynamically adjusting the reference voltage sampling point according to the P/AP state of the target cell, the resistance difference between the P-and AP states to maximize the sensing margin. Based on 28 nm CMOS and 256×256 array simulations, the DCDR scheme achieves a sensing margin of 257mV, which is more than two times that of the conventional voltage-mode sensing; the read bit-error-rate is reduced by more than 100 times to 7.99E-8; the read energy is reduced by over 30%, and the read speed is increased by 45% under the target BER of 1E-5. This work provides a high-reliability, low-power, and high-speed sensing solution for high-capacity STT-MRAM read circuits.

Han et al. from Incheon National University proposed a reliability-enhanced offset-canceling current-sampling sense amplifier (REOCCS-SA) in IEEE Transactions on Circuits and Systems–I (TCAS-I), 2026 [5]. Based on the conventional OCCS-SA structure, this circuit adds a preamplification phase and adopts a three-phase operation scheme. Meanwhile, a clamp voltage

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trimming technique is introduced to effectively improve the circuit's tolerance to offset and process variations and enhance the read reliability and stability under small signals. Simulations based on 28 nm CMOS technology demonstrate that the presented amplifier notably enhances the read yield and sensing margin, and outperforms conventional schemes in mismatch immunity, read robustness, and overall performance, providing a highly reliable read circuit solution for high-capacity STT-MRAMs.

### 2.3. Write circuit and write self-termination circuit

Intel presented a research about using 22FFL FinFET technology at the 2019 IEEE International Solid-State Circuits Conference (ISSCC) [6]. The design adopts a programmable write-verify-write (WvW) write circuit, which supports programmable write pulses, write currents, and write counts, and reduces the interconnect resistance voltage drop through dual-side write drivers in the array. This scheme makes the write current independent of the row address, effectively improving the write yield and reliability, and provides a practical solution for the write circuit design of STT-MRAMs in FinFET technology.

Jiangnan University proposed the Double-Ended Superposition Anti-Noise Write Termination scheme (DSA-WT) in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-I (2023) [7]. To address the problems of low sensing margin and poor anti-noise performance of traditional write termination schemes for STT-MRAM, the write self-termination circuit was optimized. Structurally, it integrates a sample-and-hold module, a self-biased sensing amplifier, and a Schmitt trigger, and boosts performance by superimposing the voltage variation of the bit line and source line and replacing the inverter with a dual-threshold Schmitt trigger. Experimental tests show that it achieves a 15%–33% boost in sensing margin, a 1000-fold reduction in bit error rate, and a 49.6% and 47.2% optimization in write delay and energy-delay product, respectively. Its contribution lies in solving stability problems such as early termination and signal back hopping, and providing a low-power and highly reliable write self-termination implementation scheme for high-capacity STT-MRAM.

Researchers from Peking University introduced a reliability-enhanced read circuit and a self-terminating write circuit for STT-MRAM in 16 nm FinFET [8]. The read circuit uses a two-stage charge-type sense amplifier with an accelerated reset, achieving 100% read yield and merely 92.09 fJ/bit read energy under 4.5σ resistance variation. The write circuit detects the bit-line voltage drop to terminate writing immediately after MTJ switching, reducing the write power by 82.3% at a 1ppm write error rate within 20ns. The scheme supports 1T1M high-density cells and exhibits strong robustness against process and temperature variations for on-chip cache applications.

A team from Yonsei University, Korea, proposed a dual-mode inverter-based write termination circuit (DMI-WT) for 28-nm 1T1MTJ STT-MRAM in the IEEE Journal of Solid-State Circuits (JSSC) [9]. The circuit adopts a single-ended inverter sensing structure, self-referenced offset cancellation, and Schmitt trigger design, realizing dual-mode reuse of write termination and sensing amplification, and supporting self-termination for both write 0 and write 1 operations. This doubles the effective input voltage and removes the extra area overhead. The chip measurement results show that the DMI-WT reduces the area overhead by up to 6.39× and write power by 7.5×, while improving the read/write speed and robustness. It effectively solves the problems of conventional write-termination schemes, such as large area, high power, only supporting write 1 termination, and poor robustness, providing an efficient and reliable write-termination solution for STT-MRAM.

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### 2.4. Wordline driver circuit

TSMC demonstrated a 32Mb RRAM based on the 12 nm FinFET process and presented a wordline (WL) driver circuit [10]. This circuit adopts a dual pull-up + single cascaded pull-down path structure, with separate read and write branches composed of thick-oxide IO devices and thin-oxide core devices, respectively. Functionally, it delivers a high WL voltage of over 1.5V for write operations and a low WL voltage of below 1.1V for read operations to meet the demand for fast WL activation in high-speed pipeline reading. This design resolves the conflict in WL voltage requirements between read and write operations, improves the WL rise/fall speed, reduces read/write latency, and provides critical hardware support for a high read throughput of 3.2GB/s. Its innovation lies in proposing a dual-path WL driver scheme dedicated to RRAM in advanced processes, which offers a practical reference for the collaborative design of WL drivers and high-speed read/write functions in embedded nonvolatile memories.

Samsung presented a 128Mb embedded STT-MRAM macro in 14 nm FinFET at the 2023 VLSI Symposium [11]. A gated wordline driver (GWLD) that speeds up the wordline voltage settling without adding area overhead is proposed. Together with an optimized write driver, column mux, and read offset compensation, the design reaches 18.1Mb/mm² density and 80 MHz read speed at 0.64V, achieving the best figure-of-merit The National ASIC System.

The Engineering Center of Southeast University proposed an area-efficient voltage driving scheme for high-density STT-MRAM at the 2025 IEEE 8th International Conference on Integrated Circuits, Technologies and Applications (ICTA) [12]. This work presents a Grid-Interlaced Active Word-Line Driver (GIA-WLD) structure that uses row–column decoding and 3-T transmission gate arrays to reduce the number of level shifters from O(N) to O(√N). It also introduces a Load Current Off-Chip LDO architecture that moves LDO load capacitors off-chip to reduce the on-chip area. The proposed scheme reduces the WL driver area by 3.55×, improves the memory density by 14.4%, reduces the LDO capacitor area by 88.62%, and lowers the WL charging energy by 3.5× with negligible speed degradation. This solution effectively addresses the bottleneck of excessive area overhead in dual-voltage word-line drivers and on-chip power modules for high-density STT-MRAM, providing an area-efficient word-line driving solution for large-capacity MRAM macros.

## 3. Conclusion

This paper reviews the research progress of core peripheral circuits for high-capacity STT-MRAM used in SoC applications. Focusing on three key modules, i.e., high-sensing-margin sense amplifiers, write self-termination circuits, and wordline driver circuits, it summarizes typical schemes for improving sensing margin, reducing write power consumption, enhancing driving capability, and suppressing IR-drop. The existing technologies effectively improve the read-write performance, reliability, and integration density of large-capacity arrays, providing an important reference for the application of STT-MRAM in low-power and high-density SoC, and pointing out the optimization direction for next-generation memory circuit design.

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