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Low-Power and High-Density Dynamic Random Access Memory

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Abstract. Dynamic Random-Access Memory (DRAM), as the core component of storage systems, offers a simple structure, high storage density, low unit cost, and fast read and write speeds. It is a key support for smart Internet of Things (IoT) devices to achieve low power consumption and high-density upgrades. Low-power, high-density DRAM technology has become a current research hotspot in the field of storage. In sense amplifiers, research focuses on offset compensation, noise immunity, and pre-sensing technology to improve accuracy under low-voltage operation and reduce power consumption. Using advanced Complementary Metal-Oxide-Semiconductor (CMOS) processes can reduce leakage current, lower operating voltage, and enhance process compatibility for high-density integration. 3D stacking technology breaks the physical limitations of planar DRAM through vertical integration that improves DRAM density and data retention capability. Starting from the above three major modules, this paper systematically reviews representative research achievements in low-power, high-density DRAM over the past few years. It analyzes the innovation paths and performance optimization effects of each module, and summarizes the development trends of low-power DRAM technology.

Keywords: low-power and high-density DRAM, sense amplifier, advanced CMOS process, 3D stacking technology.

1. Introduction

In the past few years, along with the ceaseless progress of Internet of Things (IoT) apparatusess, the market demand for low-power, high-density System on Chip (SoC) has been increasing, and memory is an important module of SOC chips, widely used in mobile devices, servers, portable medical devices, and other scenarios. As the core memory device in the von Neumann architecture, DRAM offers high density, and its performance directly or indirectly determines the operating efficiency of the storage system and even the entire hardware platform. Therefore, the market has put forward many requirements for Dynamic Random-Access Memory (DRAM), including the high integration degree, super low power consumption, high-speed transmission, and wide temperature stability.

Scholars at home and abroad have conducted extensive, innovative research on the core modules of low-power, high-density DRAM and, in recent years, have achieved breakthroughs in topological structure design, advanced process technologies, new device mechanisms, and 3D integration

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technology. This paper systematically reviews representative research achievements in low-power, high-density DRAM over the past few years. Based on the three dimensions of low-power sense amplifiers, DRAM based on advanced Complementary Metal-Oxide-Semiconductor (CMOS) processes, and 3D stacking technology, this paper analyzes the innovation paths and performance optimization effects of each module, summarizes the current research status and development trends of low-power, high-density DRAM, and provides a reference for subsequent research in this field.

2. High-read-accuracy sense amplifier for low-power design

The sense amplifier is the core module of the DRAM readout circuit, and its power consumption directly determines the overall read power of DRAM. Lowering the supply voltage can reduce the read power consumption of a sensitive amplifier, but if the voltage is too low, it will reduce its ability to detect and amplify weak signals, leading to decreased read accuracy and poorer circuit reliability. Therefore, it is necessary to design a sensitive amplifier with high read accuracy.

In year 2022, Tae-Bin Kim and other people put forward a noise-aware, rapid, high-efficiency offset compensation plan that is used for DRAM sense amplifiers [1]. This scheme improves the power supply noise immunity, shortens the offset compensation time, and enhances sensing reliability through maintaining the power supply circumstance unvaried in the offset compensation toward charge-sharing phase and optimizing the bitline precharge level to the shorted latch level, making it suitable for DRAM sense amplifier design schemes which are influenced by power source noise and need high-speed working.

In 2022, Pei Huang and others proposed a hybrid compensation read scheme to optimize the performance of low-voltage DRAM read operation. This scheme combines current mirror compensation, inverter switching point compensation, pre-amplified bitline voltage difference and anti-timing-jitter compensation circuit, which significantly reduces voltage mismatch, improves stability and yield, and accelerates sensing speed for low-voltage DRAM sense amplifiers [2]. This improvement was verified through a Monte Carlo simulation. Its smaller voltage mismatch can support larger memory array designs, making it suitable for for low voltage, high density, high-frequency DRAM applications.

In 2024, Li Liu and others proposed a scheme to improve DRAM sense amplifier performance by combining flip-point offset compensation, self-calibration and sensing margin enhancement [3]. This improvement is designed by comparing the limitations of three traditional sense amplifiers: offset-compensated current starved amplifier, boosted reference voltage amplifier, and inverter short-circuit calibration. Under the conditions of a 1.2V power supply, 80fF bit line load, and N:P=1:2, the FPOCSA achieves a sensing yield of 100%, a sensing speed of 6.99ns, and an area of only 8.46μm². It optimizes offset compensation capability, temperature stability, power consumption, and sensing yield at a low area cost. This makes it become the suitable thing for high-density, low-voltage, low-power DRAM chip designs.

In year 2024, Kyeongtae Nam together with other comrades put forward an offset-compensated charge-transfer pre-sensing bit-line sensitive amplifier (OC-CTPS BLSA) based on 14nm DRAM technology [4]. Without changing the charge transfer voltage, the 3-sigma window width of the charge transfer time (tct) at -25℃ and 100℃ reaches 250 ps and 500 ps, respectively, which can effectively track Vth changes and improve resistance to variations in process, voltage, and temperature (PVT). At the same time, compared with the traditional offset-compensated bitline sense amplifier (OC BLSA), it performs more stably at low voltages. This design achieves a significant reduction in failure bit rate, stable operation over a wide temperature range, and high

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robustness under low-voltage conditions, meeting the high-performance and high-volume production requirements of low-voltage DRAM.

In 2025, Changyoung Lee and others proposed an improved design for sub-1V DRAM sense amplifiers based on 25nm DRAM technology, combining ground precharge (GND PRE) configuration, charge transfer pre-sensing (CTPS) and single-ended topology [5]. This improvement has completed tape-out verification on a 256Mb DRAM chip, with very small area occupancy, requiring only 4 transistors, comparable to traditional OCSA, and without additional capacitors. At the same time, it achieves low voltage, low power consumption, and high mismatch resistance, making it suitable for sub-1V highly integrated, low-power DRAM applications.

3. DRAM based on advanced CMOS processes

As smart IoT devices increasingly demand higher density, power consumption control, and read/write performance from storage systems, DRAM, as its core component, faces technological bottlenecks in process miniaturization, while the maturity of advanced CMOS processes (such as FinFET and GAA) provides core support for technological breakthroughs in DRAM. In recent years, DRAM based on advanced CMOS technology has continuously innovated in the structure of core memory cells, innovative device design methods, and peripheral circuit optimization.

In 2020, Robert Giterman and others proposed a 1Mbit fully logic-compatible 3T gain-cell embedded DRAM in 16nm FinFET technology [6]. This study addresses leakage current in advanced processes using a mixed-threshold voltage (mixed-VT) 3T gain cell structure and achieves leakage current suppression through device type optimization and bias control. Test results indicate that this GC-eDRAM achieves a DRT of 77 μs at a 600 mV supply and 25°C, representing an improvement of more than 10 times compared to the 28nm process GC-eDRAM. At the same time, its minimum operating voltage (VDDmin) is as low as 450 mV. This device fully complies with the 16nm FinFET standard-logic design rules, requires no additional process steps, and can be directly integrated into SoCs.

In 2022, E. Capogreco and others proposed a device optimization structure based on the 14nm node process, combining RMG back-gate integration, lanthanum dipole (La-dipole) TiN/TiAl/TiN work-function metal (WFM) gate-stack optimization, and SiN cap thermal-degradation resistance [7]. It is not only compatible with high-thermal-budget manufacturing processes for FinFET and DRAM, but also significantly lowers the threshold voltage of nMOS, greatly suppresses gate leakage current, and markedly improves device thermal stability, providing a reliable solution for high-performance DRAM peripheral circuits.

In 2024, MD Yasir Bashir and others proposed a design based on the 18nm FinFET process, combining MSVL leakage current suppression and 3T/4T cell structure optimization to improve DRAM performance [8]. This improvement has been verified through comparisons with traditional 3T/4T DRAM and Sleepy Keeper architecture DRAM, showing superior overall performance across a wide voltage range of 0.5V to 1.3V.

4. 3D stacking DRAM technology

The process miniaturization of traditional planar 1T1C DRAM has approached the physical limit, and 3D stacking technology has become the core direction for increasing memory density. It achieves a leap in storage density through vertical device integration, while also addressing key issues in planar structures, such as capacitor miniaturization and increased leakage current. In recent years, 3D-stacked DRAM technology based on a capacitor-less device architecture, new channel

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materials, and advanced stacking processes has continued to innovate. The following are representative research achievements over the past few years.

In 2022, Wei-Chen Chen and others proposed a novel 3D stacked capacitorless three-word-line gate-controlled thyristor (GCT) DRAM, providing a completely new solution for 3D DRAM technology [9]. This device is transformed into a horizontal channel structure through a 90° rotation, compatible with stacked nanosheet CMOS processes and the layer-stacking technology of 3D vertical-gate NAND Flash, with a cell area of $21F^2$ per stacking layer, enabling multi-layer high-density stacking. This study addresses unselected cell interference during programming, erasing, and reading.

In 2024, Xinyi Zhu and others proposed a 3D-stacked 2T0C-DRAM based on Al_2O_3/TiO_2 heterostructure 2DEG FETs, breaking through the 3D integration bottleneck of conventional oxide devices [10]. Test results show that the device exhibits excellent electrical characteristics. At the same time, the single-layer 2T0C-DRAM cell based on this device, under dual-gate control, has a data retention time of up to 400 seconds, which is far superior to traditional Si-based DRAM (about 64 ms). This technology, through material innovation and process optimization, achieves a combination of low power consumption, long retention, and high integration, providing a new path for the application of low-power 3D-stacked DRAM.

In 2025, D. Garbin and others clarified the influence patterns and suppression conditions of the floating-body effect by using large-scale parallel transistor-array testing, TCAD simulation-assisted analysis and floating-body-effect (FBE) isolation measurement technologies, providing key support for the reliability design of the Si-based 3D DRAM architecture [11]. Its results provide key references for device design and process optimization of next-generation high-density 3D DRAM architectures (such as vertical bitline and horizontally stacked GAA), helping address reliability issues related to the floating-body effect in 3D DRAM scaling.

In 2025, N. Rassoul and others successfully demonstrated the functional integration of 3D-DRAM by adopting modular integration, simultaneous Si channel thinning and cutting, direct gate-stack deposition, and TCAD simulation scaling optimization technologies [12]. This not only enhances the vertical scalability of the device but also improves the stability of its electrical performance, providing key technical support for the mass production of high-density stacked (>100 layers) 3D-DRAM.

5. Conclusion

This paper, by reviewing recent research achievements in low-power, high-density DRAM, clarifies the core development directions, including innovations in sense amplifiers, device process evolution, 3D integration technology, and circuit performance optimization. Although low-power and high-density DRAM technology has become very mature and continues to improve in performance, the field still faces many challenges, such as inter-layer interference and process compatibility issues in 3D-stacked DRAM, the balance between retention time and endurance in new capacitor-less devices, and ensuring signal and power integrity under ultra-high-speed transmission, which remain key directions for future research. In the future, the advancement of low-power-consumption and high-density DRAM technology will further advance, achieving comprehensive improvements in power consumption, performance, density, and reliability by combining new materials and new processes, providing core support for the low-power, high-density development of next-generation storage systems, so as to meet a wider range of market demands.

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