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An Introductory Overview of Conventional CPPLL and SSPLL

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Abstract. With the development of mobile communication, intelligent healthcare, self-driving technology, and other application fields, as well as advances in IC and semiconductor devices, numerous integrated systems have imposed increasingly stringent requirements on clock signal quality. The phase-locked loop (PLL) is the mainstream architecture for clock generation at present, and PLL featuring low spur, low noise, and low power consumption has become key design objectives for researchers in recent years. Based on existing research, this paper will provide an overview of two distinct types of PLL architectures, namely the conventional charge-pump phase-locked loop (CPPLL) and the sub-sampling phase-locked loop (SSPLL), and elaborate on their relationship in terms of inheritance and evolution. By briefly introducing their operating principles, circuit architecture and operating characteristics, this paper will demonstrate the merits of SSPLL in generating low-jitter clock signals, and present some key design techniques adopted in the implementation of both types of PLLs. Through the paper, it can be concluded that the mainstream research directions for PLL improvement are mainly focused on three core aspects: the optimization design of voltage-controlled oscillator (VCO), the circuit design of the phase detector/ charge pump (PD/CP), and the dead-zone design.

Keywords: PLL, SSPLL, low noise, low spur

1. Introduction

Taking a reference signal as input, PLL is a negative feedback system that outputs a target frequency signal by achieving phase locking. PLL has a long research history: along with the birth and development of integrated circuit technology in the mid-to-late 20th century, a series of architectures, which include integrated analog phase-locked loop, frequency-multiplying phase-locked loop(FMPLL), CPPLL and fractional-N phase-locked loop (FNPLL) were proposed and developed [1]. Since the beginning of the 21st century, high-performance digitally controllable phase-locked loop architectures have been constantly developed, such as SSPLL and wideband phase-locked loops. The CPPLL is one of the most widely and thoroughly investigated PLL architectures to date. The earliest current-mode CPPLL was proposed in 1980, which is named for its charge pump module. To address the limitations caused by the unsatisfactory situation, such as the current mismatch, the SSPLL, which can achieve low phase noise and spurious performance, has received extensive attention and deep research since its invention in the early 2000s. This paper will

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sequentially introduce the operating principle and circuit architectures of these two PLL and use linear system modules to show the performance of the two types of PLL. It is expected that the paper could provide a valuable reference for PLL design, and help researchers who work in fields like integrated circuits, embedded systems, and communication transceivers to grasp the key research hotspots in this domain.

2. Charge-pump phase-locked loop

2.1. Operating principles and circuit architecture of the CPPLL

2.1.1. Operating principle of the CPPLL

Early PLL consists of a phase detector (PD), a loop filter (LF), a voltage-controlled oscillator (VCO), and a frequent divider (Divider, 1/N). Upon this architecture, the conventional charge-pump phase-locked loop (CPPLL) adopts a phase-frequency detector (PFD) to replace PD, and adds a charge pump (CP) structure at the subsequent stage, which is connected to the LF, as shown in Fig. 1.

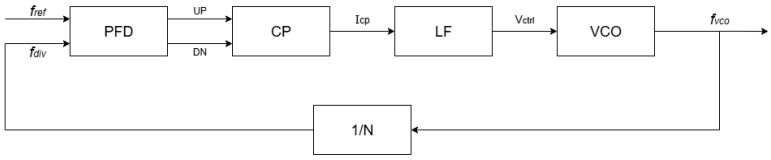


Figure 1. Block diagram of the CPPLL

The operating principle of the CPPLL can be briefly described as follows: The PFD detects the phase difference between the reference signal f_{ref} and the feedback signal f_{div} from the Divider, and outputs voltage pulse which corresponds to the phase difference. This voltage pulse controls the CP to generate corresponding output current I_{CP}. The current is filtered by the LF to suppress ripples and spurs, then converted into a control voltage V_{ctrl} to control the output frequency of the VCO. Finally, the output is fed back to the PFD through the Divider, forming a closed negative feedback loop. This closed-loop regulation process will continue until the loop achieves lock, satisfying Equation (1):

$$f_{VCO} = N \bullet f_{ref} \tag{1}$$

2.1.2. Components of the CPPLL

(1)Phase-Frequency Detector

The PDF is capable of detecting both phase differences and frequency differences between input signals. A simple PFD can be constructed by D flip-flops and basic logic gates, as shown in Fig. 2(a). The reference signal Ref and feedback signal Div work as the clock inputs of the flip-flops. For instance, as Ref leads Div, which is illustrated in Fig.2(b): when the rising edge of Ref arrives, UP=1 DN = 0; when the rising edge of Div arrives, DN = 1. At this point, the AND operating of UP and DN generates a Reset = 1, which triggers the reset operation and pulls both UP and DN back to 0 [2]. It is not difficult to spot that the width of the voltage pules output by PFD is proportional to the phase difference between the input signals.

In real design, a dead-zone problem occurs when the phase difference is excessively small, as the voltage pulse is too narrow to drive the CP [3]. To address the issue, as shown in Fig. 3, it is

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necessary to intentionally add a delay chain in the Reset path. Meanwhile, excessive delay must be avoided, as it will prolong the time which the loop using for achieving lock.

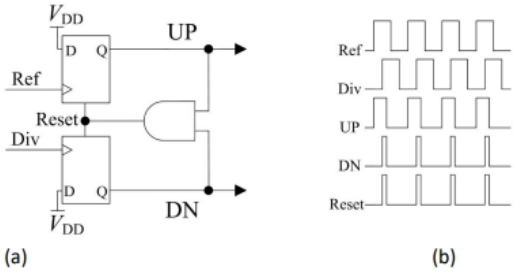


Figure 2. Circuit structure and operating timing diagram of the PFD [2]

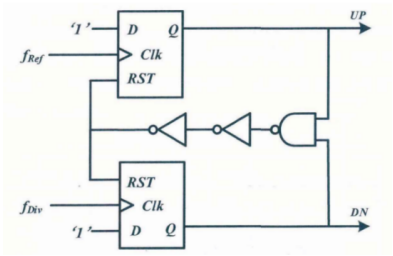


Figure 3. PFD circuit structure with an additional delay chain [1]

(2)Charge Pump

As shown in Fig. 4, the CP consists of two switches controlled by signals UP and DN, and two current sources. Its output current I_{CP} is fed into the capacitor of the LF to charge or discharge. For an ideal CP, the relationship defined in Equation (2) holds when the PLL is locked. However, in reality, a current mismatch problem ($I_{UP} \neq I_{DN}$) occurs due to the channel length modulation effect of MOS transistors. It causes a time difference in the conduction time τ of the switches for upper and lower currents sources, as shown in Fig. 5. The difference will generate ripples in the control voltage V_{ctrl} and deteriorate the performance of the VCO [2]. Furthermore, the parasitic capacitance of the switching MOS transistors will cause clock feed-through and charge-sharing issues, which will deteriorate the performance of the PLL [4].

$$I_{UP} \bullet \tau_{UP} = I_{DN} \bullet \tau_{DN} \tag{2}$$

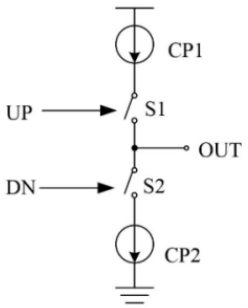


Figure 4. Circuit structure of the CP [4]

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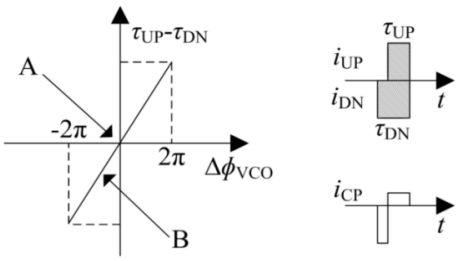


Figure 5. Current mismatch of the CP [2]

The CP is the dominant source of in-band noise in the PLL system. As illustrated in Fig. 6, to address aforementioned non-ideal effects, researchers have adopted the low-voltage cascode current mirror to suppress the channel length modulation effect by isolating the drain voltage variation of the common-source stage via the common-gate stage. Besides, complementary switching transistors can be adopted in the CP's two current source topology, so that the current sources are always connected to either the output node or the voltage follower output through a set of switches, which can avoid the charge redistribution between the parasitic capacitance of the current sources MOS transistor and the load capacitance, as the follower keeps the voltage of the two nodes consistent [4].

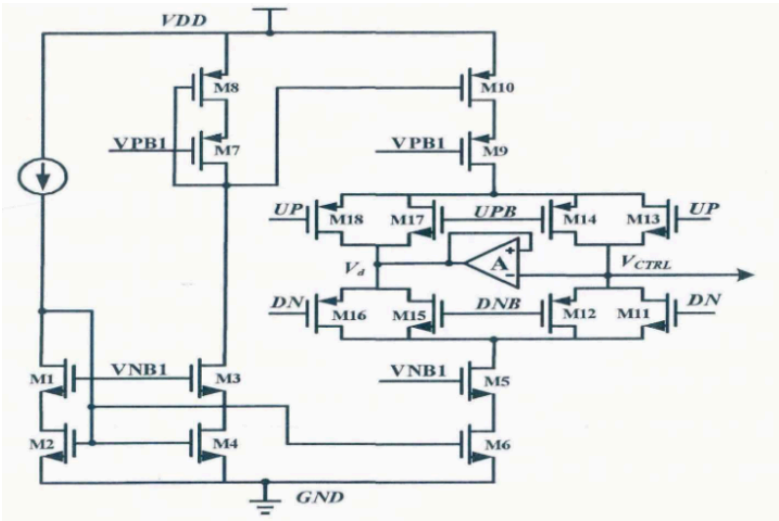


Figure 6. Circuit schematic of the Low-mismatch charge pump [1]

(3) Loop Filter

The LF is a relatively simple structure in the PLL, which is designed to suppress spurs and high-frequency components in the output of the CP and generating the V_{ctrl}. A widely used second-order LF is shown in Fig. 7 below.

To achieve sufficient phase margin, the capacitance of the series capacitor C1 is always much larger than the shunt capacitor C2. The transfer function of the filter is given in Equation 3.

$$Z_{LF}(s) = \left(R_1 + \frac{1}{C_1 s}\right) \| \left(\frac{1}{C_2 s}\right) = \frac{1+sR_1C_1}{s^2R_1C_1C_2+s(C_1+C_2)} \tag{3}$$

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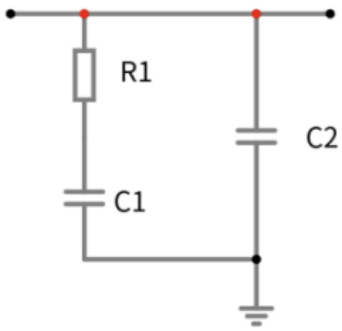


Figure 7. Second-order passive loop filter

(4) Voltage-Controlled Oscillator

A VCO is essentially a positive feedback circuit, whose model is shown in Fig. 8. The module's closed-loop transfer function can be expressed as Equation (4), and according to the Barkhausen criterion, a stable oscillation is established when the relationship defined in Equation (5) is satisfied.

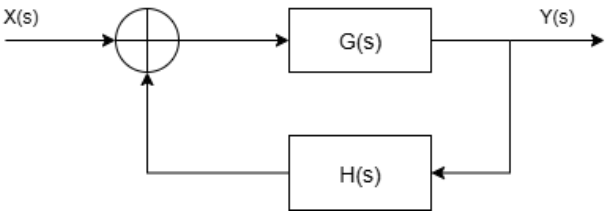


Figure 8. Feedback model

$$T\left(s\right)=\frac{G(s)}{1-G(s)H(s)} \tag{4}$$

$$|G(s)H(s)\geq 1|\ ,\ \angle G(s)H(s)=2\pi \tag{5}$$

The VCO generally consists of an LC resonant tank and a negative resistance structure which is used to compensate for the tank's energy loss. To satisfy the demand for high-performance wideband signals, the LC tank is required to have a wider tuning range, which can be achieved by the widely used switched capacitor technique, as well as the coupling transformer technique and module switching technique, received extensive attention in recent years [5].

The negative resistance structure mostly adopt cross-coupled MOS transistor configuration. As shown in Fig. 9 (a), the NMOS cross-coupled resistance structure can be equivalent to a load of $-2/g_m$, where g_m is the transconductance of the MOS transistor. In practice, designers always select an NMOS-PMOS cross-coupled resistance structure, which can provide a larger negative resistance for easier oscillation start-up [1].

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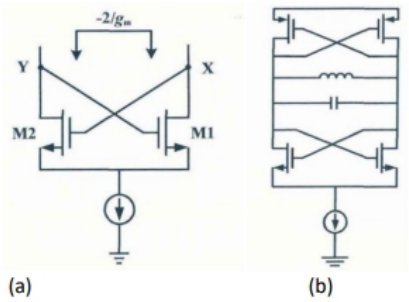


Figure 9. Cross-coupled negative resistance structure [1]

Research on VCO has become a key branch in the field of PLL research. Existing VCO-related studies cover a wide range of directions, including digitally controlled switched capacitor arrays, multi-mode oscillators, and tail-filtering resonators specifically designed for phase noise reduction, with research goals covering wide bandwidth, high efficiency, high power, and low phase noise.

(5) Frequency Divider

Divider can be categorized into integer-N frequency divider and fractional-N frequency divider. The most widely used implementation for Divider is the latch based on current-mode logic (CML), as shown in Fig. 10 [1].

A CML circuit consists of an upper-stage differential pair and latch cell, as well as a lower-stage differential clock pair and current source. Benefiting from its fully symmetric differential architecture, it exhibits excellent common-mode noise immunity. However, its inherent quiescent current results in relatively high power consumption, while also enabling its higher operating speed.

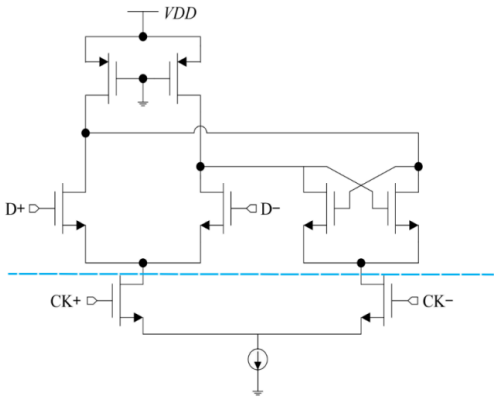


Figure 10. CML circuit structure [2]

2.2. Loop analysis of the CPPLL

2.2.1. Linear model of the CPPLL

As described in the previous sections, the CP is activated and operates only when its switches are turned on by the voltage pulses from PFD, thus PFD/CP is inherently a discrete system. However, for loop analysis, the PFD/CP system can be approximately considered as a linear circuit when the loop is in the locked state, with its transfer function given by Equation (6), where C is the capacitor for the charging and discharging of the CP output current [1].

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$$H_{PFD/CP}(s) = \frac{v_{ctrl}}{\Delta\phi} = \frac{I_{CP}}{2\pi Cs} = K_{PD}\frac{1}{Cs} \tag{6}$$

Similarly, the tuning gain characteristic of the VCO can also be regarded as linear, with its transfer function given in Equation (7), where K_{VCO} is the linear tuning gain of the VCO.

$$H_{VCO}(s) = \frac{K_{VCO}}{s} \tag{7}$$

Finally, according to Fig. 11, the open-loop transfer function of PLL presented in Equation (8):

$$H_{open}(s) = \frac{K_{PD}Z_{LF}K_{VCO}}{Ns} \tag{8}$$

And the closed-loop transfer function presented in Equation (9):

$$H_{closed}(s) = \frac{H_{open}(s)}{1+H_{open}(s)} \tag{9}$$

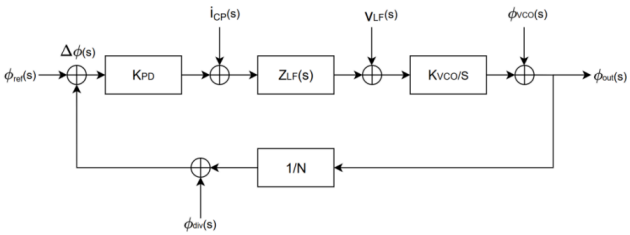


Figure 11. Linear Phase-domain model of the CPPLL

2.2.2. Phase noise of the CPPLL

The noise of the CPPLL can be categorized into in-band noise and out-of-band noise. The in-band noise is dominated by the reference signal, PFD/CP and Divider, while the out-of-band noise is mainly contributed by the VCO. The corresponding noise module is shown in Fig. 12 and Table 1 summarizes the transfer functions and characteristics of the dominant noise sources.

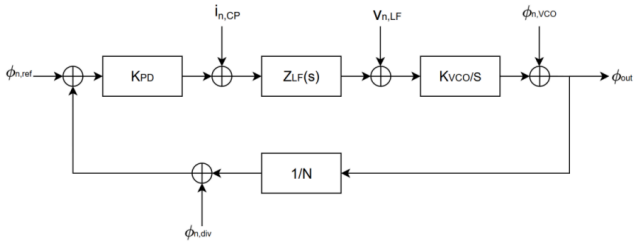


Figure 12. Loop noise model of the CPPLL

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Table 1. Transfer functions and characteristics for PLL noise sources

Noise Source	Transfer Function	Characteristic
reference input	$\frac{\phi_{out}(s)}{\phi_{ref}(s)} = \frac{NH_{open}(s)}{1+H_{open}(s)}$	low-pass
PFD/CP	$\frac{\phi_{out}(s)}{i_{CP}(s)} = \frac{N}{K_{PD}} \frac{H_{open}(s)}{1+H_{open}(s)}$	low-pass
loop filter	$\frac{\phi_{out}(s)}{v_{LF}(s)} = \frac{K_{VCO}}{s} \frac{1}{1+H_{open}(s)}$	band-pass
VCO	$\frac{\phi_{out}(s)}{\phi_{VCO}(s)} = \frac{1}{1+H_{open}(s)}$	high-pass
divider	$\frac{\phi_{out}(s)}{\phi_{div}(s)} = \frac{NH_{open}(s)}{1+H_{open}(s)}$	low-pass

In the noise analysis of VCO, Leeson's phase noise model is a well-established classic model [6]. As shown in Fig. 13, the model divides the phase noise spectrum into three distinct regions, namely the $1/f^3$, $1/f^2$ and $1/f$, which are sequentially induced by up-converted flicker noise of MOS transistors, thermal noise from MOS transistor and the resonant network, and noise from peripheral circuits and substrate. It can be expressed by Equation (10), where P_ω denotes the output signal power, F is the noise factor, and $\Delta\omega_{1/f^3}$ represents the corner frequency between $1/f^3$, $1/f^2$ regions [1].

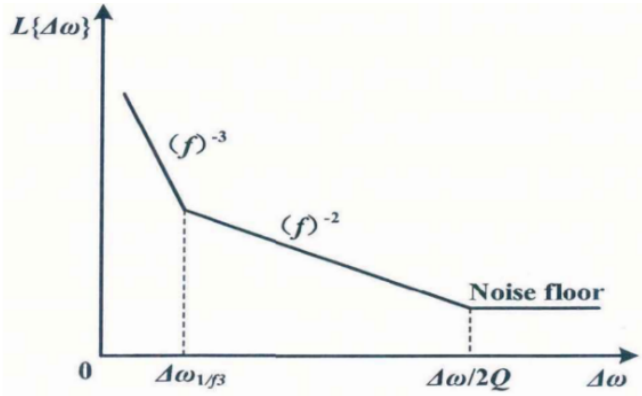


Figure 13. Leeson's phase noise model [1]

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$$L\left\{\Delta\omega\right\} = 10\log\left[\frac{2FKT}{P_\omega}\left[1+\left(\frac{\omega}{2Q\Delta\omega}\right)^2\right]\left(1+\frac{\Delta\omega_{1/f^3}}{\Delta\omega}\right)\right] \tag{10}$$

Of additional note here is the impact of the Divider on the noise performance. With $\beta_{PFD,CP} = \frac{K_{PD}}{N}$ defined, the in-band noise contributed by the CP can be expressed as shown in Equation (11), where $S_{n,i_{CP}}$ is the power spectral density of the current noise from the CP [7]. It can be seen that the noise power of the CP is amplified by a factor of N^2 due to the Divider.

$$L_{CP} \approx \frac{1}{2} S_{n,i_{CP}} \left| \frac{\phi_{out}(s)}{i_{CP}(s)} \right|^2 \tag{11}$$

3. Sub-sampling phase-locked loop

3.1. Operating principle and architecture of SSPLL

3.1.1. Operating principle of SSPLL

The structure shown in Fig. 14 is a SSPLL with a dead zone, which is also a classic SSPLL topology. In contrast with the CPPLL, the SSPLL consists of two parts: a core loop and a frequency-locked loop (FLL). The core loop is composed of a sub-sampling phase detector (SSPD), a sub-sampling charge pump (SSCP), a pulse generator (Pulser), as well as the LF and the VCO shared with the FLL [8].

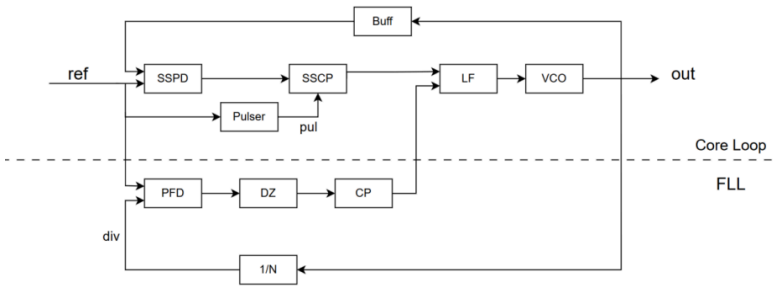


Figure 14. Block diagram of the SSPLL

The operating principle of the SSPLL is as follows: When the PLL is activated in the out-of-lock state, the two core loops and the FLL operate simultaneously until the phase difference between div and ref is sufficiently, and $f_{VCO} = N \bullet f_{div}$ is satisfied. The FLL then enters the dead zone and stops operating, leaving the core loop to work alone until the loop is fully locked. If the FLL exits in the dead zone, the two loops will resume operation simultaneously.

3.1.2. Components of the SSPLL

Since many modules, such as the LF and VCO, are similar to those of the CPPLL, only the unique structures of the SSPLL are briefly introduced here.

(1) SSPD, SSCP and Pulse Generator

The term "sub-sampling" describes the process in which the low-frequency reference signal f_{ref} is used to sampling the high-frequency signal f_{VCO}. Fig 15 shows the schematic of the SSPD/CP and Pulser. The reference signal Ref samples the VCO feedback signal to control the charging and

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discharging of the sampling capacitor C_{sam}, which sets the voltage V_{sam} and further regulates the magnitude of the I_{UP} and I_{DN}. In other words, the output currents of the SSCP is determined by the amplitude of V_{sam}.

When the SSPLL is locked, the rising edge of Ref is aligned with the zero-crossing point of the VCO output, where $V_{sam+} = V_{sam-}$, resulting in $I_{UP} = I_{DN}$ and $i_{CP} = 0$[1]. To ensure the FLL dominates when the two loops operate simultaneously, the SSCP current is generally set smaller than the CP current in the FLL.

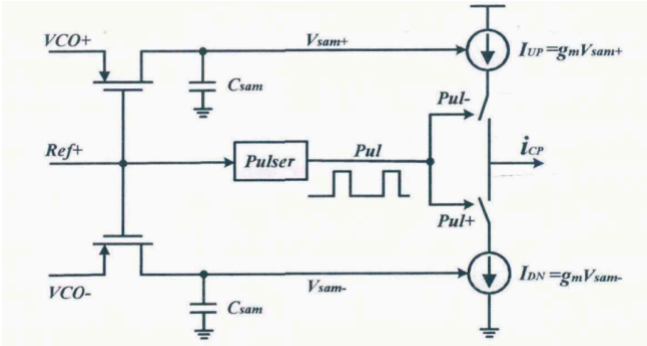


Figure 15. Circuit structure of the SSPD/CP [1]

(2) Dead Zone

As indicated by the aforementioned operating principle, a dead zone is required in the SSPLL's FLL to disable the loop upon frequency lock, thereby avoiding the noise contribution from the Divider. The dead zone settling is critical: an excessively narrow dead zone will cause system lock loss, as phase noise of the high-gain VCO, reference clock jitter, and inherent quantization error may make the phase noise error exceed the SSPD capture range when the core loop operates alone. In contrast, an overly wide dead zone will force the core loop to start operating independently from a situation with a large phase difference, leading to a longer locking time. Therefore, a narrow dead zone ensuring a reliable capture range is highly desired in practical design.

To solve the above issues, controllable dead zone designs have been investigated. As shown in Fig. 16, this PFD structure with a tunable narrow dead zone is implemented with simple gate circuits and D flip-flops, and its dead zone width can be adjusted by controlling the delay via the external tuning voltage V_{TUNE}[2].

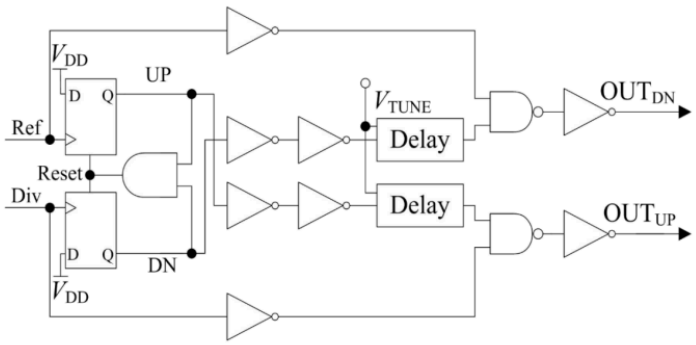


Figure 16. PFD design with dead zone [2]

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3.2. Loop analysis of the SSPLL

3.2.1. Linear model of the SSPLL

The linear and noise model of the SSPLL is shown in Fig. 17

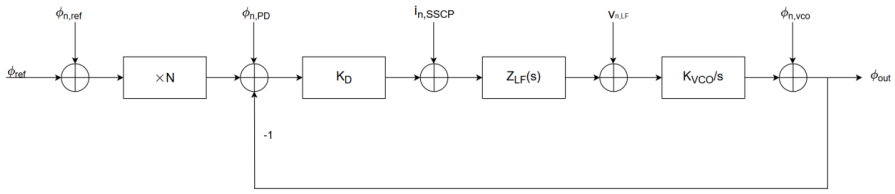


Figure 17. Linear and noise model of the SSPLL

In the locked state, for ease of analysis, let the VCO output be $V_{VCO} = A_{VCO}\sin(2\pi f_{VCO} + \theta_{VCO})$. The small-signal of the SSPD/CP is presented in Equation (12):

$$\beta_{SSPD/CP} = K_D = K_{SSPD} \bullet K_{SSCP} = \frac{\Delta V_{sum}}{\Delta \phi} \bullet \frac{\Delta I_{CP}}{\Delta V_{sum}} = \frac{A_{VCO}\sin(\Delta \phi)}{\Delta \phi} \bullet g_m \approx A_{VCO} g_m \tag{12}$$

For the sub-sampling structure in Fig. 15, the SSPD uses differential sampling, with a Pulser controlling the on/off switching of the SSCP. Assuming that the SSCP is turned on for a duration of τ_{ref} within one reference period T_{ref} , the small-signal gain of the SSPD/CP is given by Equation (13):

$$\beta_{SSPD/CP} = 2A_{VCO} g_m \frac{\tau_{ref}}{T_{ref}} \tag{13}$$

Similar to the CPPLL, the open-loop transfer function of the SSPLL is expressed in Equation (14):

$$H_{open}\left(s\right) = \frac{K_D Z_{LF} K_{VCO}}{s} \tag{14}$$

3.2.2. Performance of the SSPLL

(1) Phase Noise of the SSPLL

From Equation (6) and Equation (12), the ratio of the feedback gains of the two PD/CP structures can be obtained as shown in Equation (15). It can be readily seen that this value is much greater than 1, which means that the SSPLL exhibits a significantly stronger suppression capability for charge pump noise [5].

$$\frac{\beta_{SSPD/CP}}{\beta_{PFD/CP}} = \frac{2\pi \bullet N \bullet A_{VCO} \bullet g_m}{I_{CP}} \tag{15}$$

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Table 2. Transfer functions and characteristics for SSPLL noise sources

Noise Source	Transfer Function	Characteristic
reference input	$\frac{\phi_{out}(s)}{\phi_{ref}(s)} = \frac{NH_{open}(s)}{1+H_{open}(s)}$	low-pass
SSPD/CP	$\frac{\phi_{out}(s)}{i_{SSCP}(s)} = \frac{1}{K_D}\frac{H_{open}(s)}{1+H_{open}(s)}$	low-pass
loop filter	$\frac{\phi_{out}(s)}{v_{LF}(s)} = \frac{K_{VCO}}{s}\frac{1}{1+H_{open}(s)}$	band-pass
VCO	$\frac{\phi_{out}(s)}{\phi_{VCO}(s)} = \frac{1}{1+H_{open}(s)}$	high-pass

(2)Reference Spurs of the SSPLL

A critical issue in the SSPLL is that periodic sampling of the VCO signal by the SSPD causes periodic variations in the VCO load, leading to the binary frequency shift keying (BFSK) effect. This effect generates output spurs in the PLL, as formulated in Equation (16), where M_{ref} is the duty cycle of the reference signal, and C is the total capacitance of the LC resonant tank in the VCO [5].

$$SP_{fref,BFSK,SSPLL} = 20\log\left[\sin\left(\pi \bullet M_{ref}\right) \bullet \frac{N}{2\pi} \bullet \frac{C_{sum}}{C}\right] \tag{16}$$

This issue can be resolved by adding a complementary SSPD structure that performs sampling with a half-period offset from the original SSPD, to keep the VCO load constant.

4. Conclusion

This paper briefly outlines the operating principles, module architectures, and loop linear module analysis of both the CPPLL and the SSPLL. Primarily introductory in nature, this work does not cover the specific design of a certain PLL, nor the quantitative analysis of practical module design. The performance analysis mainly focuses on phase noise, with limited discussion on other aspects, which need further elaboration.

Overall, driven by the demand for high-performance PLL, low-noise and low-jitter PLL have become the research hotspot in recent years. Core designs including CP, oscillator and PDF dead zone optimization are the key to reducing non-idealities and improving PLL performance. In addition, due to the inherent performance trade-offs of PLL, achieving lower power consumption and higher efficiency while guaranteeing high-quality signal output is undoubtedly a critical research direction in the future.

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