Proceedings of CONF-MSS 2026 Syposium: Mechanical Control and Automation
DOI: 10.54254/2755-2721/2026.BJ32635

Review of Theoretical Characteristics, Influencing Factors, and Low-Power Applications of MOSFETs in the Subthreshold Region

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Abstract. With the boom of IoT, neuromorphic computing, and implantable biomedical electronics, ultra-low-power integrated circuit design is a critical focus. Operating MOSFETs in the subthreshold region offers a practical solution via exponential drain current–gate voltage dependence, enabling ultra-low-power operation. However, subthreshold behavior is strongly influenced by physical and technological factors, complicating the reliable design of devices and circuits. This paper reviews MOSFET subthreshold operation from a device-physics perspective. It explores subthreshold conduction physics, emphasizing diffusion-dominated transport and the exponential current–voltage relationship. A core current model is analyzed to clarify key parameters, such as the thermal voltage and gate-channel coupling efficiency. The impacts of temperature, device structure, fabrication processes, and material properties on subthreshold characteristics are discussed, along with representative low-power analog modules and applications, including IoT sensing and neuromorphic computing. This work finds that thermal effects, electrostatic control, and material-dependent carrier behavior determine subthreshold performance. Integrating device physics, characteristic modulation, and applications into a unified framework, it provides design insights and highlights challenges for robust ultra-low-power system development.

Keywords: Subthreshold Region, Low-Power Electronics, Analog Circuits, MOSFET

1. Introduction

The rapid proliferation of Internet-of-Things (IoT) devices, neuromorphic computing systems, and implantable biomedical electronics has significantly increased the demand for ultra-low-power integrated circuits. In these emerging applications, electronic systems are often required to operate continuously while relying on severely constrained energy sources, such as miniature batteries or energy-harvesting units. Under such conditions, minimizing power consumption becomes a dominant design objective, frequently outweighing traditional performance metrics such as operating speed or throughput. This imperative is rooted in a fundamental physical challenge: the scaling of the supply voltage in ultra-large-scale integrated circuits cannot keep pace with the

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DOI: 10.54254/2755-2721/2026.BJ32635

continued miniaturization of transistors, a limitation often referred to as the "Boltzmann tyranny" [1].

To meet these stringent energy requirements, subthreshold MOSFET operation has attracted growing attention as an effective strategy for achieving ultra-low power consumption in applications with low to moderate performance demands [2]. In the subthreshold region, circuit functionality is enabled by the exponential dependence of drain current on gate voltage below the threshold voltage, allowing operation at extremely low supply voltages and current levels. This regime is therefore well-suited for always-on and low-frequency applications such as sensor interfaces, biomedical signal processing, and bio-inspired computing systems. Despite notable advances in subthreshold circuit techniques and compact modeling, subthreshold behavior remains highly sensitive to temperature variations, device structure, and fabrication-related parameters, which poses challenges for robustness and predictability.

This paper reviews the operation of a MOSFET in the subthreshold region from a device- and physics-orientated viewpoint. We first discuss the characteristics of subthreshold conduction, and then briefly review how environmental factors, device structure, process parameters and material properties affect subthreshold qualities. By linking device-level mechanisms with circuit-level implications, this review aims to support future developments in energy-constrained electronic systems and to guide more robust subthreshold design strategies.

2. Fundamental theory of subthreshold MOSFET operation

2.1. Physical nature of subthreshold region

The subthreshold region of a MOSFET, also referred to as the weak inversion region, is defined by the condition where the gate-to-source voltage (VGS) is lower than the threshold voltage (VT) but greater than zero. In this operating regime, the transistor is biased below its threshold voltage, and circuit functionality relies on the device's subthreshold leakage current [3]. Unlike a strong inversion operation, where a high-density inversion layer enables carrier transport dominated by drift under a transverse electric field, subthreshold conduction is governed primarily by diffusion current [4]. From a physical perspective, the defining feature of subthreshold operation is the exponential dependence of the channel carrier concentration on the surface potential. As the gate-source voltage increases, the surface potential rises approximately linearly, leading to an exponential growth in the minority-carrier density at the semiconductor–oxide interface. Consequently, the drain current exhibits an exponential dependence on VGS, in contrast to the quasi-linear behavior observed in strong inversion.

This diffusion current is fundamentally driven by the steep concentration gradient of minority carriers between the source and the weakly inverted channel. The gate voltage indirectly controls this process by modulating the surface potential. Its efficiency is weakened by the capacitance divider formed by the oxide layer capacitance (COX) and the depletion layer capacitance (Cdep). This attenuation is quantified by the slope factor (where $\kappa = COX / (COX + Cdep) < 1$), which directly determines the efficiency of the gate in controlling the surface potential. Thus, the sub-threshold region represents a transitional state in which the mobile carrier density increases exponentially with the surface potential, yet remains low enough not to form a conductive channel dominated by drift. This is in sharp contrast to the strong inversion state, where Cdep becomes negligible, and the gate can directly control the high-density inversion layer.

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2.2. Core subthreshold current model

When a MOSFET operates in the subthreshold region, the drain current is dominated by diffusion rather than drift [5]. Under this condition, the drain current can be expressed in an exponential form that explicitly captures its dependence on gate voltage, temperature, and electrostatic coupling, and is commonly written as

$$I_{DS}=I_0 e^{\left(\frac{\kappa(V_{GS}-V_T)}{U_T}\right)}\left(1-e^{-\frac{V_{ds}}{U_T}}\right)\left(1+\frac{V_{ds}}{V_E}\right) \quad (1)$$

The parameter I0, known as the subthreshold leakage current, is typically set at 10^{-14} A. It represents the reference drain current when VGS equals the threshold voltage VT, reflecting the effective carrier transport capability of the device. UT is defined as the thermal voltage, expressed as $\frac{kT}{q}$ (where k denotes the Boltzmann constant, T is the absolute temperature, and q is the elementary charge). At room temperature (approximately 300 K), UT is conventionally taken as 25 mV. This parameter characterizes the influence of thermal excitation on carrier diffusion, linking the subthreshold current to temperature. The parameter κ represents the gate-to-channel coupling efficiency and is defined as κ = COX / (COX + Cdep) with values smaller than unity due to the presence of depletion capacitance.

For $\left(1-e^{-\frac{V_{ds}}{U_T}}\right)$, this part describes the dependence of the sub-threshold current on the drain-source voltage Vds. When Vds reaches a certain level (typically Vds > 4UT), $e^{-\frac{V_{ds}}{U_T}}$ approaches 0, and at this point, this part can be approximated as 1. In this situation, the drain voltage no longer significantly affects the current. The device enters sub-threshold saturation For $\left(1+\frac{V_{ds}}{V_E}\right)$, in this part, VE represents the early voltage, which reflects the channel length modulation effect (that is, an increase in Vds will shorten the effective channel length). For long-channel MOSFETs, the value of VE is relatively large, while Vds is limited to a smaller value in the sub-threshold region. The ratio of Vds to VE is small (much less than 1), and this formula is approximately equal to 1 in part. In this situation, channel-length modulation can be disregarded. Ultimately, this current formula is simplified to

$$I_{DS}=I_0 e^{\left(\frac{\kappa(V_{GS}-V_T)}{U_T}\right)} \quad (2)$$

This condensed expression represents the most commonly utilized form for analyzing subthreshold low-power circuits.

3. Critical influencing factors of subthreshold characteristics

3.1. Environmental factor: temperature dependence

Temperature is one of the most critical environmental factors influencing the subthreshold characteristics of MOSFETs. Unlike a strong inversion operation, where temperature effects are mainly associated with mobility degradation, subthreshold conduction is dominated by thermally activated diffusion. Consequently, the drain current in the subthreshold region shows a strong temperature dependence.

From a physical perspective, subthreshold conduction arises when carriers thermally surmount the potential barrier between the source and the channel. This mechanism is reflected in the thermal

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voltage UT = $\frac{kT}{q}$, which appears in the exponential term of the subthreshold current expression. Since UT increases linearly with absolute temperature, temperature directly modulates the exponential relationship between IDS and VGS. As the temperature rises, the sensitivity of the drain current to the gate voltage is reduced, weakening gate control under a given bias condition.

Temperature also affects subthreshold behavior by influencing the subthreshold swing (SS). Theoretically, SS is proportional to temperature [6]. Although the slope factor κ , determined by the capacitive coupling between the oxide capacitance and the depletion capacitance exhibits only weak temperature dependence, the increase in UT leads to a larger subthreshold swing at elevated temperatures. This implies that a greater change in gate voltage is required to achieve the same order-of-magnitude variation in drain current.

3.2. Device structure and process

The subthreshold characteristics of MOSFETs are strongly influenced by device geometry and fabrication parameters, which determine the electrostatic control of the gate over the channel potential in the weak inversion regime. Because the drain current depends exponentially on the surface potential, structural and process variations exert a more pronounced impact than in strong inversion operation.

Channel length is a primary structural factor affecting subthreshold behavior. In long-channel devices, the source-to-channel potential barrier is predominantly controlled by the gate voltage, resulting in well-defined exponential IDS-VGS characteristics. As the channel length decreases, the drain electric field increasingly penetrates the channel region, lowering the effective barrier height even when VGS < VT. This leads to increased subthreshold leakage and enhanced drain-induced barrier lowering (DIBL), which can be interpreted as a drain-voltage-dependent shift of the threshold voltage in the subthreshold current model [7]. The severity of DIBL is further influenced by temperature, being reduced under cryogenic conditions [8].

Channel width mainly scales the magnitude of the subthreshold current rather than altering its slope. Since diffusion current in weak inversion is proportional to the effective channel width, wider devices exhibit larger absolute current for a given gate bias, while preserving the exponential dependence on VGS. Therefore, in the subthreshold regime, the drain current scales approximately with W/L, , maintaining its exponential gate-voltage dependence [7].

The gate oxide thickness is a critical process parameter that directly affects the gate-to-channel coupling efficiency through the oxide capacitance, Cox. A thinner oxide increases Cox, thereby enhancing the coupling factor κ . Alternatively, the use of high-κ gate dielectric materials is a practical approach to increase gate capacitance and strengthen capacitive coupling, thereby improving subthreshold performance parameters and switching behavior [9,10]. In the subthreshold regime, this stronger coupling enables more efficient modulation of the surface potential by the gate voltage, resulting in a steeper subthreshold slope and improved current controllability. Conversely, thicker gate oxides weaken electrostatic control, increasing the sensitivity of subthreshold current to substrate and drain bias.

Substrate structure and doping profiles further influence subthreshold performance by shaping the depletion behavior beneath the channel. In bulk MOSFETs, the depletion region introduces a finite capacitance Cdep, which reduces gate control efficiency. Fully depleted structures mitigate this effect by suppressing Cdep, thereby improving subthreshold swing and reducing leakage.

Doping concentration and spatial distribution also affect both the threshold voltage and depletion capacitance. Higher doping increases Cdep, degrading the subthreshold slope, while non-uniform

DOI: 10.54254/2755-2721/2026.BJ32635

doping can induce local potential fluctuations. Due to the exponential sensitivity of subthreshold current to barrier height, such variations significantly impact leakage and device variability. As a result, lightly doped or carefully engineered doping profiles are often preferred for subthreshold-oriented device designs.

3.3. Material properties

Material properties primarily influence subthreshold characteristics through the semiconductor channel and the gate dielectric, as these components determine carrier statistics and electrostatic control in the weak-inversion regime. Because subthreshold conduction relies on thermally activated carriers, material-dependent effects are amplified compared with strong inversion operation.

The semiconductor channel material affects subthreshold behavior mainly through its intrinsic carrier concentration and band structure. Since the surface carrier density is exponentially related to surface potential, materials with higher intrinsic carrier concentration generate more thermally excited minority carriers, increasing the subthreshold drain current at a given gate bias. While the exponential dependence on VGS remains unchanged, the absolute current level in weak inversion is strongly material-dependent.

The gate dielectric material critically determines interface quality and electrostatic stability. Interface states at the dielectric–semiconductor boundary introduce charge trapping mechanisms that distort the gate-voltage-to-surface-potential relationship. In the subthreshold regime, where carrier density is low, such traps significantly degrade gate control, resulting in increased subthreshold swing and current variability. Modeling studies indicate that an interface trap density on the order of 2×1012 cm-2 is sufficient to induce anomalous subthreshold swing behavior [11]. In addition, fixed charges within the gate dielectric shift the effective threshold voltage, which directly affects the exponential term in the subthreshold current model.

4. Representative low-power application scenarios

4.1. Basic analog functional modules

The exponential current-voltage relationship and high transconductance efficiency of subthreshold MOSFETs enable the implementation of fundamental, ultra-low-power analog building blocks. These modules form the core of energy-constrained systems by performing essential functions such as biasing, amplification, and computation with minimal power.

A primary application lies in current sources and current mirrors. A transistor biased in subthreshold saturation can generate stable nanoampere-level currents determined by its gate voltage. By connecting the gates of matched devices, precise current mirrors can be implemented, providing an efficient means of bias distribution across integrated circuits; indeed, temperature-insensitive current and voltage references are critical for the stable operation of integrated circuits across various applications [12]. Moreover, the high transconductance efficiency enables energy-efficient amplifiers. Operational and transconductance amplifiers operating in subthreshold can achieve significant voltage gain with bias currents of only a few nanoamperes. To maintain high gain, devices must operate in saturation, which typically requires VDS > 100 mV in subthreshold conditions. This makes them ideal for the first stage of signal conditioning in sensor interfaces and biomedical systems, where both signal amplitude and available power are extremely small.

Most distinctively, the exponential IDS - VGS law allows the transistor to function as a native analog computational unit. A single device can directly perform logarithmic or exponential

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transformations between its current and voltage. By interconnecting transistors in specific configurations, circuits that execute multiplication, division, and other nonlinear operations can be realized entirely in the analog domain. This enables feature extraction and signal compression directly at the sensor node, bypassing the high overhead of analog-to-digital conversion and digital processing for simple tasks. These basic functional modules collectively establish the analog foundation upon which more complex low-power systems, such as neuromorphic processors, are built.

4.2. Emerging application scenarios

The analog building blocks enabled by subthreshold operation are particularly suited to two major application domains: the Internet of Things (IoT) and neuromorphic computing. Both require extreme energy efficiency, making subthreshold operation a natural choice. This suitability arises from the intrinsic characteristics of subthreshold MOSFETs, including ultra-low operating current and favorable subthreshold swing, which support stable operation under strict power constraints.

In IoT and Edge Sensing, the primary challenge is achieving years of battery life or even energy autonomy through harvesting. This challenge is underscored by the fundamental constraint that IoT sensor nodes must operate for long lifetimes on limited battery capacity, making energy efficiency a paramount design concern. Subthreshold circuits enable system-on-chip implementations operating at nanowatt-to-microwatt power levels, covering sensor interfaces, analog front-ends, and low-frequency digital control logic. By operating digital circuits in the subthreshold or near-threshold region, dynamic power consumption is significantly reduced. Combined with duty-cycling strategies —where the system remains in a low-leakage sleep state and activates only for brief sensing or transmission events—overall energy consumption can be minimized. Nanoampere-level biasing and subthreshold timing circuits are key enablers of this approach, supporting applications such as remote monitoring, implantable medical devices, and distributed sensor nodes.

In neuromorphic computing, the device physics of subthreshold MOSFETs closely resemble the behavior of biological neurons. The exponential IDS–VGS relationship parallels the nonlinear activation characteristics of neurons, making subthreshold devices well-suited for spiking neural networks (SNNs). Furthermore, a transistor operating in the linear region with small VDS behaves as a voltage-controlled analog resistor, enabling compact implementations of programmable synaptic weights. Subthreshold circuits can achieve extremely low standby power, enabling large-scale networks of "neurons" and "synapses" to operate in an event-driven manner. Because SNNs rely on sparse spike-based signaling, analog computation in this regime reduces the need for frequent analog-to-digital conversion and high-energy digital multiplication. Experimental demonstrations of subthreshold neuromorphic hardware have reported substantial improvements in energy efficiency compared with conventional digital implementations.

5. Conclusion

This paper comprehensively examines the core aspects of MOSFET operation in the subthreshold region. First, the physical mechanism of subthreshold conduction is clarified as diffusion-dominated carrier transport, fundamentally different from the drift-dominated behavior in strong inversion, with the exponential IDS-VGS relationship serving as the theoretical foundation. Second, key influencing factors—including temperature, device structure, process parameters, and material properties—are systematically analyzed. Temperature primarily affects the thermal voltage and subthreshold swing, device-level optimizations enhance electrostatic control and mitigate short-channel effects, and

DOI: 10.54254/2755-2721/2026.BJ32635

appropriate material selection helps suppress leakage and variability. Third, these characteristics are shown to enable efficient realization of ultra-low-power analog building blocks and to support emerging applications such as IoT edge sensing and neuromorphic computing systems. The review's key significance lies in proposing a unified framework that connects scattered research and lays a theoretical foundation for the wider adoption of subthreshold technology in emerging low-power scenarios. However, this study has limitations: it focuses on theoretical analysis with insufficient experimental validation using actual circuit data, making it difficult to verify the consistency between theoretical and actual performance. Additionally, some analyses remain preliminary and superficial, limiting its practical engineering applicability.

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