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Design of Low-Power Systems Based on Neuromorphic Computing

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Abstract. With the rapid advancement of the Internet of Things and edge intelligent computing, the demand for low-power, high-energy-efficient computing systems has become increasingly urgent. The traditional von Neumann architecture suffers from poor energy efficiency in data-intensive tasks due to the 'memory wall' problem. Neuromorphic computing, as an emerging paradigm that mimics the biological brain's information-processing methods, offers highly promising solutions to overcome energy-efficiency bottlenecks through event-driven operations, integrated sensing, storage, and computation, and novel devices such as memristors. This paper systematically analyses and summarises the latest research achievements in neuromorphic computing across hardware devices, system architectures, and optimisation strategies. It first presents fundamental hardware implementation options for simulating neurons and synapses, highlighting memristors' benefits in low-power synaptic plasticity. Then the system-level low-power architectures are discussed-including the event-driven paradigm and compute-in-memory concept integration. Finally, taking IoT edge nodes as an example application scenario of energy-efficient neuromorphic systems, it also outlines current major issues confronting technologies along with future development directions.

Keywords: Neuromorphic computing, Low-power systems, memristors, Event-driven, Compute-in-memory

1. Introduction

The traditional digital computer is based on Boolean logic and the Von Neumann architecture. The transistor, which acts mainly as a switch, forms the basic element of this structure where storage is separated from processing units. There exists huge power consumption overheads in such data-intensive operations like AI inference because of frequent movement or transfer of data between different locations (known as 'memory wall' problem). This becomes more apparent with resource-constrained IoT edge devices and mobile terminals.

To address this challenge, researchers have turned their attention to nature's most efficient known computational system: the biological brain. The brain's information processing exhibits event-driven, highly parallel, and compute-in-memory characteristics, achieving extraordinary energy efficiency. For equivalent functionalities, digital computers typically consume energy levels several orders of magnitude higher. Neuromorphic computing, the practice of mimicking the brain, aims to

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replicate its structure and operational principles, with neurons and synapses serving as its core computational units. Consequently, the primary task in neuromorphic electronics is to discover or design electronic devices capable of simulating these biological elements, thereby enabling the construction of entirely novel computational systems.

This paper systematically reviews low-power neuromorphic computing design techniques. Firstly, it delves into core hardware technologies for simulating neurons and synapses. Secondly, it analyses system architectures and optimisation strategies tailored for low power consumption. Thirdly, it evaluates performance through Internet of Things application scenarios. Finally, it summarises existing achievements and challenges, and outlines future research directions.

2. Core hardware and low-power mechanisms for neuromorphic computing

The foundation for realising neuromorphic computing lies in physical devices capable of simulating biological neuron and synapse behaviour. The characteristics of these devices directly determine the system's power consumption, integration density, and performance.

2.1. Simulating neurons

The function of a neuron is to integrate input signals and generate a discharge (spike pulse) upon reaching a threshold. Approaches implemented through electronic circuits include:

Integrated Operational Amplifier Circuits: Use of capacitors, resistors, and operational amplifiers in building differential equation circuits for accurately simulating the process of membrane charge-discharge (integration) and its spike-firing behavior. This method was used in some early and is also being used in a few modern neuromorphic chips (for example Intel's Loihi), this provide high accuracy but relatively large circuit area is required.

Dedicated spike circuits: Complex CMOS circuits are designed to directly implement simplified neuronal models, such as the Integrate-and-Fire (I&F) model or the more intricate Izhikevich model. This approach facilitates greater scalability and is commonly used to realise high-density neuronal arrays.

2.2. Analogue synapses

Synapses are responsible for storing connection weights and performing weighted computations, making them pivotal in determining system power consumption and area requirements.

Digital Memory + Digital-to-Analogue Converter (DAC): This represents the most direct approach, storing synaptic weights in digital memory (such as SRAM) and converting them via a DAC into analogue current or voltage for multiply-accumulate operations. However, this approach requires extensive digital circuitry and conversion units, resulting in substantial area and power overhead that can become a bottleneck for large-scale integration [1].

Memristors: Among the most revolutionary neuromorphic devices, memristors are two-terminal devices whose resistance depends on the cumulative charge flow or the voltage applied historically. This property perfectly aligns with the biological synapse's characteristic of 'connection strength varying with activity history'.By applying voltage pulses of different polarity and amplitude, the value of the resistor can be set in two directions (high resistance states as weak connections, low resistance states as strong connections) thereby enabling synaptic plasticity e.g. STDP (Spike-Timing-Dependent Plasticity) [2]. Memristor cross-arrays can physically implement vector-matrix

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multiplication, inherently supporting in-memory computing and drastically reducing computational power consumption.

Frontier Advancements: Diffusive memristors achieve extreme miniaturisation and low power consumption by physically emulating ion diffusion processes in biological neurons. For instance, research at the University of Southern California has realised an artificial neuron requiring only a single transistor (approximately 4 μm^2), with power consumption projected to be several orders of magnitude lower than conventional designs [3]. Furthermore, biomimetic neurons based on two-dimensional materials (such as MoS_2) integrate perception, memory, and computation into a 'three-in-one' architecture. At the single-device level, this approach overcomes the von Neumann bottleneck, achieving power consumption that is over 1000 times lower than that of conventional CMOS devices [2].

3. System architecture and optimisation strategies for low power consumption

Low-power components alone are insufficient to constitute an efficient system; systematic architectural optimisation is required.

3.1. Event-driven paradigm

Event-driven operation forms the cornerstone of neuromorphic computing's low-power implementation. Unlike traditional systems that use synchronous clocks and fixed sampling rates, event-driven systems activate and process data only when meaningful changes occur.

Operating Principle: At the sensor level, techniques such as level-crossing ADCs (LC-ADCs) are employed [4], sampling the input signal only once when its amplitude exceeds a preset threshold, thereby generating an 'event'. At the processor level, neurons within spiking neural networks (SNNs) perform computations and discharge only upon receiving sufficiently strong input spikes.

Fundamental Advantage: The system's dynamic power consumption correlates directly with signal activity. When inputs are static or change slowly, most circuits remain dormant, consuming only minimal static power. This confers unparalleled energy efficiency when processing sparse events.

3.2. System-level optimisation techniques

Sensing-Storage-Computing Integration: Integrating sensing, storage, and computation within a single device or tightly coupled units fundamentally eliminates data movement. For instance, a one-step magnetron sputtering process of MoS_2, two-dimensional material simultaneously depositing electrodes and creating defects achieve photoelectrically coordinated synaptic plasticity in biomimetic synapse transistors [5]. This hints at the sensing-storage-processing capabilities that could be integrated features to make system-level power consumption lower, hence quite likely for use in such applications.

Parallel and Pipeline Architectures: In SNN accelerator design, CONVP units fuse convolution and pooling operations to minimise intermediate data access [6]. Concurrently, inter-output parallelism enables layer-to-layer pipelining, where previous layer outputs are fed to subsequent layers immediately, reducing cache requirements and processing latency.

Computational Precision Optimisation: While maintaining application performance, quantising network weights and activation values from 32-bit floating-point to 8-bit or lower fixed-point significantly reduces memory capacity requirements and computational unit power consumption.

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3.3. Specialised processing circuits

Within system construction, dedicated circuits such as Winner-Take-All (WTA) / Loser-Take-All (LTA) are frequently employed for decision-making and attention mechanisms. Architectural selection is critical based on application requirements: [7]

Current Transfer Device (CTD) Architecture: Suitable for high-speed, high-resolution scenarios with few input channels.

Binary Tree Architecture: Suitable for high-precision scenarios with numerous input channels.

Time-Domain Architecture: Balances compact structure, high speed, and moderate resolution, suitable for multi-input scenarios.

4. Application scenarios and performance evaluation

4.1. System design concept

(1) Perception Layer: Employ event-driven sensors, such as brain-inspired visual devices [8], which generate pulse events only upon detecting scene changes (e.g., moving objects), rather than continuously outputting video streams.

(2) Processing Layer: Deploy locally an SNN processor implemented using memristor arrays or FPGAs. This processor performs real-time, low-power inference (e.g., gesture recognition, anomaly detection) on incoming event streams.

(3) Communication Layer: High-power wireless communication modules (e.g., Wi-Fi or LoRa) are activated solely when the processing layer detects significant events (e.g., recognition of specific gestures) to upload results to the cloud.

4.2. Performance evaluation

Compared to traditional systems based on MCUs and digital signal processing, neuromorphic systems offer substantial energy-efficiency advantages for such intermittent tasks. Key comparative metrics include:

Average power consumption: Neuromorphic systems can operate at the microwatt level, whereas traditional systems typically exceed the milliwatt range.

Energy per inference: A critical efficiency metric (unit: Joules per inference). Published neuromorphic implementations achieve 10-100 times greater efficiency than conventional approaches.

Inference latency: Neuromorphic systems generally exhibit lower response delays due to local processing and event-driven characteristics.

4.3. Common application scenarios

The integration of neuromorphic computing with event-driven architectures is particularly suited to scenarios demanding high real-time performance, low power consumption, and intermittent responsiveness:

(1) Event-based Camera

An event-based camera is a sensor inspired by biological vision that generates asynchronous 'event' outputs solely in response to changes in pixel brightness, rather than fixed-frame-rate images like conventional cameras [9].This characteristic confers significant advantages in scenarios involving high-speed motion and high dynamic range. For instance:

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Autonomous Driving and Drone Obstacle Avoidance: At high speeds, event cameras are capable of detecting moving objects instantly with minimal delay in microseconds and consumption of power at a small fraction compared to conventional vision systems. The applications range from vehicles to pedestrians.

Industrial Inspection: Anomalies in products or machines on fast production lines-event-driven processing removes massive redundancy within the information making real-time detection feasible efficiently.

(2) Insect-inspired Robotics

Drawing upon the efficient perception and decision-making mechanisms of insect nervous systems, neuromorphic systems enable autonomous navigation and interaction with exceptionally low power consumption:

Micro autonomous robots: These are the kind of robots which can run for a long time in resource-constrained environments—say, battery powered or an unstructured environment like a post-disaster search and rescue scenario. The event camera records output only when there is change detected within its field of view; hence low power consumption suited perfectly to such applications. Equipped with obstacle avoidance and target tracking(by SNN processor) capabilities.

Swarm intelligence:(Combination between both systems)—many micro autonomous robots communicating/collaborating together as one system via events detected either from changes within their environment or new task requirements imposed suddenly on them by some external agent.

(3) 24-Hour Ambulatory Cardiovascular Monitoring

Conventional wearables often exhibit high power consumption due to continuous data collection and transmission. Neuromorphic systems enable intelligent monitoring through event-driven approaches:

Real-time Abnormal Heart Rhythm Detection: Local SNN processors continuously analyse electrocardiogram signals, triggering recordings or remote alerts only when arrhythmias are detected (e.g., ventricular premature beats, atrial fibrillation), thereby avoiding redundant data transmission.

Long-Term Health Tracking: Integrating multi-modal event sensing (e.g., blood oxygen, blood pressure) enables round-the-clock low-power monitoring, particularly suited for elderly patients or post-operative rehabilitation management.

5. Conclusion

This paper systematically analyses the design of low-power neuromorphic computing systems. Research indicates that neuromorphic computing offers a robust technical pathway to address energy efficiency bottlenecks in edge computing through a series of innovative technologies, including novel devices such as memristors, event-driven paradigms, and compute-in-memory architectures.

Key findings are summarised as follows:

At the device level, emerging components such as memristors and two-dimensional materials not only enable low-power synaptic and neuronal functions but also lay the groundwork for system-level energy-efficiency gains through functional integration.

At the architectural level, event-driven processing and compute-in-memory fundamentally reduce unnecessary data movement and computation, while optimisation techniques like parallel pipelines further enhance computational efficiency.

At the system level, co-design approaches tailored to specific scenarios, such as the Internet of Things, demonstrate neuromorphic systems' significant advantages in energy efficiency and latency.

Current technology faces hurdles in commercialization and pilot deployment. Device-level issues like resistance fluctuation and limited element lifetime persist. Manufacturing bottlenecks include

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CMOS compatibility and yield improvement. System-level design lacks efficient toolchains, and hardware/software co-design is complex. Future work involves 2D materials, carbon nanotubes for devices, ASI-ARCH AI hardware design, and heterogeneous integration of neuromorphic units with conventional systems to enhance energy efficiency in edge computing.

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