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Low-Power CMOS Integrated Circuit Design Technology: A Review from Process Optimization to Architectural Innovation

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Abstract. Moore's Law has spurred the continuous scaling of CMOS integrated circuits for decades, yet the ensuing power consumption bottleneck has severely restricted the development of mobile, IoT and portable electronics. This paper presents a systematic literature review of low-power CMOS design technology from 1990 to the present, aiming to sort out its evolution from process-level optimization to architecture-level innovation and offer theoretical references for next-gen ultra-low-power chip design. Using literature and comparative analysis, it combs the core technologies and achievements of two key stages and analyzes the driving forces of process and application changes. The study finds the technology has shifted distinctly from early device/circuit-level optimization to later system/architecture-level innovation, with the synergy of process tech, application demand and academic research as its core driving force. It also points out that future design will focus on the power-performance-cost balance under sustainable computing, with reconfigurable architecture and AI-based power optimization as key research directions.

Keywords: Low-power CMOS, Process optimization, Architectural innovation, Integrated circuit design

1. Introduction

Complementary Metal-Oxide-Semiconductor (CMOS) technology is the foundation of modern electronics and integrated circuits and has long developed following Moore's Law, which states that the density of integrated circuits doubles every two years [1]. As transistor feature sizes shrink, chip performance and density improve significantly, but power consumption density rises sharply, causing heat dissipation and power supply challenges. These issues restrict further CMOS development, especially for battery-powered mobile, IoT, and wearable devices.

Since the 1990s, extensive low-power CMOS research has been conducted, with techniques such as voltage scaling, power gating, and near-threshold computing widely studied. However, most work focuses on individual technologies or specific process nodes, lacking a systematic review of the full evolutionary context and the relationships among technological progress, application requirements, and innovations. This study aims to fill this gap by clarifying the evolution and driving forces of low-power CMOS design over the past 30 years.

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Based on literature analysis and comparative analysis, this paper reviews low-power CMOS technologies from the 1990s to the present. It reveals evolutionary patterns and technical characteristics across stages, supplements the missing systematic overview, and predicts future trends. This work provides theoretical support and technical guidance for ultra-low-power chip design in the AIoT era.

2. Development context of low-power CMOS integrated circuit design technology

The development of low-power CMOS integrated circuit design technology has obvious stage characteristics. According to the core driving force, technical research focus and application background, its development process can be divided into two key stages: the early process-driven stage (1990–2010) and the architectural innovation stage (2010–2020). Each stage has formed a distinctive technical system and application achievements according to the process level and market demand at that time and laid a solid foundation for the subsequent development of the technology.

2.1. Early process-driven stage (1990–2010)

From 1990 to 2010, the development of CMOS technology was mainly driven by the scaling of process nodes, and the research on low-power design was also focused on device-level and circuit-level process parameter optimization. In this stage, the feature size of CMOS transistors shrank from the micron level to the nanometer level, and the bulk silicon process was the mainstream technical solution. The core problem faced by low-power design was to reduce the dynamic power consumption of circuits and suppress the leakage power consumption caused by process scaling, and the three core technical directions formed were voltage scaling, threshold voltage adjustment and leakage current suppression technology [2].

2.1.1. Core technologies: voltage scaling, threshold voltage adjustment, and leakage current suppression technology

Voltage scaling is the most direct and effective low-power design method in this stage, which is based on the basic principle that the dynamic power consumption of CMOS circuits is proportional to the square of the supply voltage. By appropriately reducing the supply voltage under the premise of meeting the basic performance requirements of the circuit, the dynamic power consumption of the chip can be reduced in a square relationship. Threshold voltage adjustment technology optimizes the electrical characteristics of transistors by adjusting the threshold voltage of MOS transistors: increasing the threshold voltage can effectively reduce the off-state leakage current of transistors, while reducing the threshold voltage can improve the driving capability of transistors and the operating speed of circuits. This technology realizes the balance between circuit performance and leakage power consumption by adjusting the threshold voltage according to different application requirements. Leakage current suppression technology is aimed at the problem of increasing leakage power consumption with the shrinking of transistor feature size, and adopts technical means such as channel doping adjustment, gate oxide thickness optimization and reverse body bias to reduce the various leakage currents in transistors, including subthreshold leakage, gate leakage and junction leakage [3].

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2.1.2. Representative achievements: subthreshold design based on bulk silicon process and dynamic power consumption optimization methods

The representative research achievements of the process-driven stage are the subthreshold design and dynamic power consumption optimization methods based on the bulk silicon process. Subthreshold design realizes the ultra-low power operation of the circuit by operating the transistor in the subthreshold region, where the transistor works in the weak inversion region, and the supply voltage is lower than the threshold voltage of the transistor. This design method can reduce the power consumption of the circuit to the nanowatt or microwatt level, which is especially suitable for low-speed, low-power sensor nodes and portable electronic devices with strict power consumption requirements. Dynamic power consumption optimization methods form a complete optimization system including clock tree optimization, signal activity reduction and power supply voltage partitioning, which reduce the dynamic power consumption of the circuit by reducing the switching frequency of transistors, the number of switching transistors and the supply voltage of different circuit modules. These technical achievements have been widely applied in the design of early mobile phone chips, low-power microcontrollers and embedded systems, and laid the basic technical framework for low-power CMOS design.

2.2. Architectural innovation stage (2010–2020)

After 2010, with the gradual slowing down of Moore's Law and the rapid development of mobile Internet, IoT and wearable device technologies, the demand for ultra-low-power chips in the market has increased sharply, and the application scenarios of CMOS chips have become more diversified and complex. The single device-level and circuit-level process optimization can no longer meet the increasingly stringent power consumption requirements of chips, and the low-power CMOS design technology has thus entered the architectural innovation stage driven by application demand [4]. In this stage, the mainstream process nodes developed from 90nm to 7nm, FinFET (Fin Field-Effect Transistor) technology replaced the traditional bulk silicon planar process and became the mainstream technical solution, and the research focus of low-power design shifted from process optimization to system-level and architectural-level innovative design.

2.2.1. Core technologies: power gating, clock gating, Dynamic Voltage and Frequency Scaling (DVFS), and Near-Threshold Computing (NTC)

The core technologies formed in the architectural innovation stage include power gating, clock gating, dynamic voltage and frequency scaling (DVFS) and near-threshold computing (NTC), which construct a multi-level low-power optimization system from circuit to system. Power gating technology realizes the power supply cut-off of the idle module in the chip by adding a power switch transistor between the power supply and the circuit module, which fundamentally eliminates the leakage power consumption of the idle module and is one of the most effective technologies for reducing the static power consumption of the chip. Clock gating technology reduces the switching power consumption of the clock tree by closing the clock signal of the idle circuit module, because the clock tree is the part with the highest power consumption in the digital circuit, and closing the clock signal of the idle module can significantly reduce the dynamic power consumption of the chip. DVFS technology adjusts the supply voltage and operating frequency of the chip in real time according to the actual load and computing requirements of the chip, realizing the dynamic balance between power consumption and performance: when the computing load is low, the supply voltage

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and operating frequency are reduced to save power consumption; when the computing load is high, the supply voltage and operating frequency are increased to meet the performance requirements [5]. Near-threshold computing is an important technical innovation in this stage, which operates the transistor in the near-threshold region (the supply voltage is slightly higher than the threshold voltage of the transistor), making a better balance between power consumption and performance than subthreshold design, and can realize high-performance computing under low power consumption conditions, which is suitable for the design of low-power computing chips with certain performance requirements.

2.2.2. Representative achievements: power management based on multi-core architecture and the design of ultra-low-power sensor nodes

Typical applications in this stage are multi-core-based power management and ultra-low-power sensor nodes. Multi-core power management uses dynamic core activation, load balancing, and heterogeneous cores to optimize overall chip power, improving resource efficiency and reducing waste. It is widely used in smartphone SoCs, tablets, and servers, boosting power-performance efficiency. Architecture-driven ultra-low-power sensor nodes integrate microcontrollers, wireless modules, and sensors with multiple low-power techniques, enabling long standby times. This hardware foundation supported large-scale IoT deployment and industry growth [6].

3. Analysis of key nodes in the evolution of low-power CMOS design technology

Low-power CMOS design technology evolves non-linearly, driven jointly by advancing process nodes and changing application scenarios. Scaling process nodes provides the hardware foundation and technical space for low-power design innovations, while diverse, customized application demands act as the core impetus for the technology's transformation and upgrading. This section analyzes key evolution nodes of low-power CMOS design technology from these two perspectives and assesses its future development trends by integrating the latest technological advances.

3.1. Impact of process node evolution

CMOS process node scaling is a foundational driver of low-power design technology. Scaling from 90nm to 7nm has shrunk transistor feature sizes, boosted chip integration density, and reshaped chip electrical characteristics, power density and performance—posing new low-power design challenges while spurring technological innovation. As shown in Table 1, as CMOS processes scale from 0.18 μm to 65 nm, the FoM (a key metric for power-performance efficiency) generally improves, with values dropping from 1125.0 fJ/step to 514.3 fJ/step, indicating better energy efficiency. However, power per column (μW/col) does not strictly decrease; for example, 65 nm (383 μW/col) is higher than 0.18 μm (128 μW/col). This shows that while advanced processes enhance energy efficiency per step, power density can rise due to higher integration density, requiring careful design optimization [7].

Table 1. Performance comparison under different process nodes

ADC type	SS ADC	SS ADC	SS ADC	SS ADC	SS ADC	SS ADC	SS+TDC	SS+TDC
Process	0.11 μm	65nm	0.11 μm	0.11 μm	0.18 μm	0.13 μm	0.11 μm	0.11 μm
Resolution (bits)	12	12	10	11	12	12	12	12
1-H time [μs]	7.4	5.5	4	7	36	3.7	2.44	2

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Table 1. (continued)

Power [μW/col]	366	383	76	--	128	400	129-198	187
FoM [fJ/step]	661.2	514.3	296.9	--	1125.0	361.3	196.6	182.6

Moreover, the 7nm FinFET technology reconfigured planar transistors into 3D fin structures, enhancing gate control, cutting subthreshold leakage, and further elevating power-performance ratios. Next-gen GAA technology will feature a fully surrounding 3D gate structure, boost gate control and lay a new hardware foundation for ultra-low-power CMOS design.

Process node advancement optimizes device-level electrical properties and fuels circuit and system-level low-power design innovations. FinFET's strong leakage suppression enhances power gating efficiency, while the high integration of advanced processes enables multi-core architectures, heterogeneous integration and 3D packaging—expanding technical space for architectural-level power optimization. In short, process node evolution and low-power design innovation are mutually reinforcing, with process technology serving as the critical hardware foundation for the ongoing development of low-power CMOS design [7].

3.2. Technological transformation driven by application scenarios

Changing application scenarios are the core driver of low-power CMOS design evolution. Since 2010, the rapid growth of mobile Internet, IoT, wearables, and AIoT has diversified chip applications and raised stricter demands for power, size, and battery life. This shift has pushed low-power design from process optimization to architecture innovation and encouraged integration with AI and edge computing.

Smartphones demand both high performance and low power. This has driven advances in DVFS, multi-core power management, and heterogeneous architectures, forming a complete low-power design system for mobile SoCs [8]. Wearables require ultra-low power and miniaturization, supported by subthreshold design, power gating, ultra-low-frequency operation, and energy harvesting to enable long standby times.

AIoT combines AI and IoT, requiring edge computing with ultra-low power. Unlike cloud computing, edge computing processes data locally, reducing communication power, latency, and security risks. This has spurred the integration of near-threshold computing and AI accelerators, becoming a key research direction for energy-efficient edge AI hardware [9].

3.3. Analysis of future development trends

Under sustainable computing and the growth of AIoT, edge, and quantum computing, low-power CMOS design faces new opportunities and challenges. Its future focuses on balancing power, performance, and cost, integrating reconfigurable architectures, AI-based power optimization, and 3D packaging/heterogeneous integration—shifting from single technical tweaks to systematic design with full-lifecycle power optimization.

Reconfigurable low-power architectures adjust hardware structure and resources in real time to match loads, eliminating redundant power waste. FPGA-ASIC fused designs combine flexibility and efficiency, fitting AIoT's diverse needs. AI-based power optimization applies machine learning/deep learning throughout chips' lifecycle: optimizing design-stage layout and architecture, and dynamically adjusting voltage, frequency, and resources in application to adapt to real-time loads [10].

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3D packaging (via TSV) boosts integration and cuts interconnection power, while heterogeneous integration combines diverse chips for system-level optimization. Both bring challenges like high heat flux, requiring advanced power, thermal, and signal integrity management. Additionally, sustainable computing drives full-lifecycle power optimization (design to recycling), with environmental sustainability as a key indicator. Balancing power, performance, and cost remains core, with low-power design moving toward intelligence, systematization, and sustainability.

4. Conclusion

This paper conducts a systematic literature review on low-power CMOS integrated circuit design technology from 1990 to the present, sorting out its development from a process-driven stage to an architectural innovation stage and analyzing key evolution nodes driven by process scaling and application changes.

The research concludes that low-power CMOS design has clearly transformed from device/circuit-level process optimization to system/architecture-level innovation; the collaborative drive of process technology, application demand and academic research is its core power. Process scaling (90nm to 7nm) provides a hardware foundation, while mobile, wearable and AIoT demands promote architectural innovation, and academic research supports technical exploration.

However, this paper has limitations: it lacks in-depth research and comparative analysis of emerging low-power technologies (e.g., energy harvesting, neuromorphic computing) and only adopts the literature review method without experimental verification or data analysis of low-power technology in actual chip design cases.

Future research can focus on balancing power, performance and cost under sustainable computing, including an in-depth study of reconfigurable architectures and AI-based optimization, cross-integration with AIoT/edge computing, and establishing a full-lifecycle low-power design system for chips.

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