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A Review of CNTFETs: Mechanisms, Manufacturing, and Why They Are a Promising Alternative to Silicon MOSFETs

Alex Zha

Palo Alto High School, Palo Alto, USA
azha0109@outlook.com

Abstract. Due to the approaching physical limit of MOSFET scaling resulting from factors including short-channel effect in this post-Moore era, new forms of transistors that exhibit different mechanisms of operation from traditional silicon MOSFETs are gaining increasing attention in research and industry. Among them, the Carbon Nanotube Field-Effect Transistors (CNTFETs), devices that use a Carbon Nanotube as the channel between source and drain, are commonly viewed as promising alternatives. The most common type of Carbon Nanotube used, and the focus of this review, is Single-Walled Carbon Nanotubes (SWCNTs) formed from graphene sheets that are rolled into a cylindrical shape. This manuscript will first cover the basic structure and mechanism of the SWCNTs and CNTFETs – focusing on how CNT's thin channel can potentially mitigate challenges in scaling by minimizing the short-channel effect of silicon MOSFETs, while maintaining or improving other properties, including a higher carrier mobility and lower power usage. Then, the detailed process of manufacturing would be presented, together with a discussion on the extent to which CNT's tube-like structure and impurities are challenged to deposit onto large wafers, preventing it from mass production. Finally, there would be a brief analysis of the future implications of CNTFETs.

Keywords: Carbon Nanotube Field-Effect Transistors, Semiconductor material, Carbon Nanotube, Transistor scaling

1. Introduction

Transistors are the basic components of the computer chips. The development of Complementary Metal Oxide Semiconductor (CMOS) has been following Moore's law for several decades. Moore's law is an industrial trend which states that the number of transistors that can be integrated on a chip tends to double roughly every two years. Historically, this is largely done by shrinking the size of transistors [1].

However, as the size of transistors reaches the nanoscale, the continued shrinking of transistor size does not provide proportional improvement for the whole chip performance and efficiency as it used to. One of the issues is that silicon Metal Oxide Semiconductor Field Effect Transistor (MOSFET), building units of CMOS, suffers significant short channel effects at decreasing channel lengths. The short channel effects happen when the channel length becomes comparable to the

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source/drain depletion regions. This effect causes problems like the drain-induced barrier lowering and increasing off-state leakage, which affects MOSFET performance [2].

The difficulty in MOSFET scaling has motivated the development of new forms of transistors that exhibit different mechanisms of operation from traditional silicon MOSFETs.

2. Carbon nanotube field-effect transistors

2.1. Carbon nanotube

Carbon nanotubes are tubes of graphene sheets rolled into a cylindrical shape. The size of a carbon nanotube is on the nano scale, the diameter typically ranging from 0.4 to 3 nm [3].

A single-wall carbon nanotube is one that is made from a single-layer graphene sheet. The atomic arrangement of the carbon-carbon bonds is described by chirality, labeled by indices(n,m), which specify the direction that the graphene is wrapped. Figure1 shows the structure of each type of CNT.

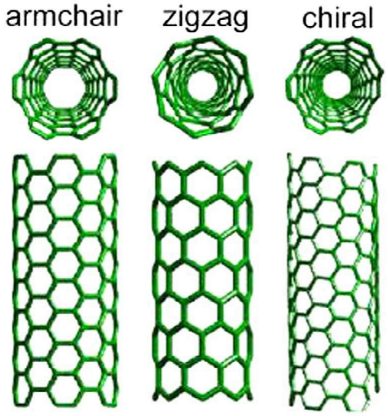

Figure 1. Different types of CNT [4]

All arm-char ones are metallic; those with n-m ≡ 0 (mod3) are nearly metallic or sometimes considered as semiconductors with small band gaps; and all other ones are semiconductors, and the band gap is inversely proportional to the diameter. (0.8 eV for a tube with a diameter of 1 nm.) [5].

Thus, by controlling the chirality of the carbon nanotube, one can obtain semiconducting nanotubes with desired band gaps.

2.2. CNTFET structure

The CNTFET overall structure is similar to the MOSFET, with source, drain, gate, and one or more semiconducting channels. There are several types of CNTFET, including Back-Gated CNT, Top-Gated CNTFET, Wrap-around gate CNTFETs, and Suspended CNTFETs [6]. The main difference is the position and the shape of the gate. The source and drain of the CNTFET are connected by one or more carbon nanotubes, acting as channels. The gate is placed near the CNT between the source and drain.

2.3. CNTFET mechanism

There are three types of CNTFET mechanisms according to Marani, R [7]: 1. Schottky Barrier (SB) CNTFET 2. Partially-Gated (PG) CNTFET 3. MOS-like CNTFET (also known as C-CNTFET). Schottky Barrier CNTFET(SB-CNTFET)

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When the two metals (source and drain) touch the CNT, there's a mismatch of the energy levels between the metal's Fermi level and the band edges of the CNT, called the Schottky barrier.

For example, Figure 2 shows a p-doping SB-CNTFET, when there is no gate voltage, the valence band edge is lower than the metal's Fermi level. This means that there is a thick barrier width that acts like a wall, blocking the hole from flowing through. When applying a voltage on the gate, the electric field created affects the band edge of the CNT, by increasing the energy level of the valence band, making the wall thinner so the hole can more easily tunnel through the barrier

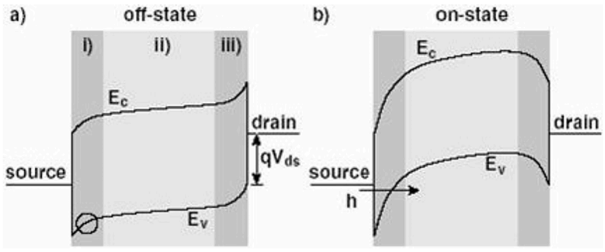

Figure 2. The band diagram and the direction of the hole in a p-doped SB-CNTFET

2.3.1. Partially-Gated CNTFET (PG-CNTFET)

PG-CNTFET uses ohmic source/drain contact, through which carriers can easily enter the nanotube from the source and exit from the drain without significant barriers. If the CNT is doped, when there is no gate voltage, the device is on; when the gate voltage is applied, the electric field blocks the flow of charge carriers in the nanotube by depleting the carriers in the gated region. If CNT is intrinsic(undoped), it is normally off, and the gate voltage induces carriers to carry the current flow.

2.3.2. MOS-like CNTFET (C-CNTFET)

With Source and drain doped, the MOS-like-CNT, also known as the conventional CNTFETs(C-CNTFETs), follows the same mechanism as silicon MOSFETs, where gate voltage controls the carrier density of the whole CNT.

2.4. Advantages of CNTFET over CMOS

2.4.1. Minimizing the short channel effect

Because the MOSFET has a relatively thick channel body, the gate can't control the channel everywhere perfectly [8]. When you shrink the channel length too much, the electric field induced by the drain voltage could have a strong influence on some part of the channel, which makes it likely to experience the Drain Induced Barrier Lowering (DIBL), increasing off-state leakage.

This DIBL also happens in CNTFET. However, because of CNTFETs' ultra-thin diameter, the electric field of the gate voltage can reach the entire part of the CNT better than in the MOSFET, meaning it can have better control. Specifically, in the model mentioned by Tan et al., the DIBL of CNTFET is 40.85mV/V and MOSFET is 83.89mV/V, indicating a significantly smaller DIBL in CNTFET under their comparison condition [9].

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2.4.2. High carrier mobility

Carrier mobility refers to the ability of charge carriers to go through a semiconductor without being scattered. CNTFET provides better carrier mobility. In Zhang et.al.'s 2025 paper, their paper shows that the theoretical values of CNTFET's carrier mobility reach up to 105 cm2·V−1·s−1, far exceeding those of silicon (1400 cm2·V−1·s−1) [3].

2.4.3. Power consumption

In their 2025 paper, Pan and Chen cite prior experimental data showing that CNTFET half adders can reduce power consumption compared with CMOS half adders. Specifically, within an operating voltage between 0.8V and 1.2V, the power consumption of the CNTFET half adder is reduced by 73% [10].

3. Manufacturing

3.1. Steps for manufacturing

3.1.1. CNT preparation

Figure 3, part a) describes the step of CNT chemical vapor deposition (CVD) [11]:

Before step 1: Prepare a nanodiamond (ND) particle and put it on a SiO_2 wafer.
Step 1: Purified the ND by heating the air
Step 2: Keep heating the ND with noble gas to turn the sp3 carbon to sp2 carbon.
Step 3: initial growth: add carbon gases to grow the cap
Step 4: Keep increasing the temperature
Step 5: Secondary growth: keep feeding carbon gases and (H_2O) if used to continue growth

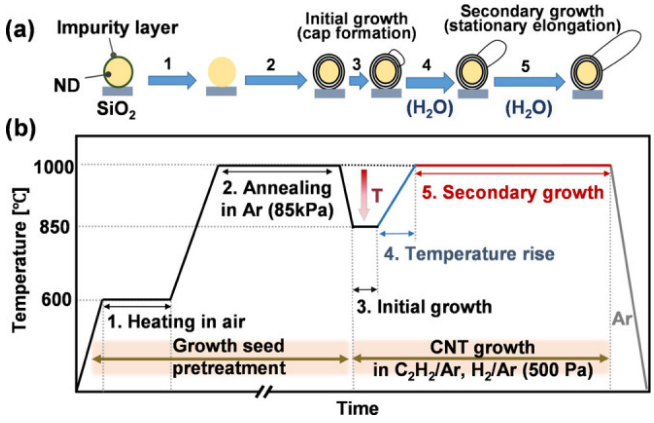

Figure 3. Part a) schematic diagram of the growth of SWCNTs by CVD [11]

3.1.2. Manufacturing CNTFET

Figure 4 describes the steps of a back-gate CNTFET fabrication [12]:

1. Use thermal oxidize to form SiO_2 dielectric layer on both sides of the Si wafer
2. Spin coating the photoresist on the top side of wafer
3. Remove SiO_2 on the back side of the wafer using etching
4. Deposit CNT onto the top side of the wafer.

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5. Use the shadow mask to locate the source and drain, and deposit metals (metallization)

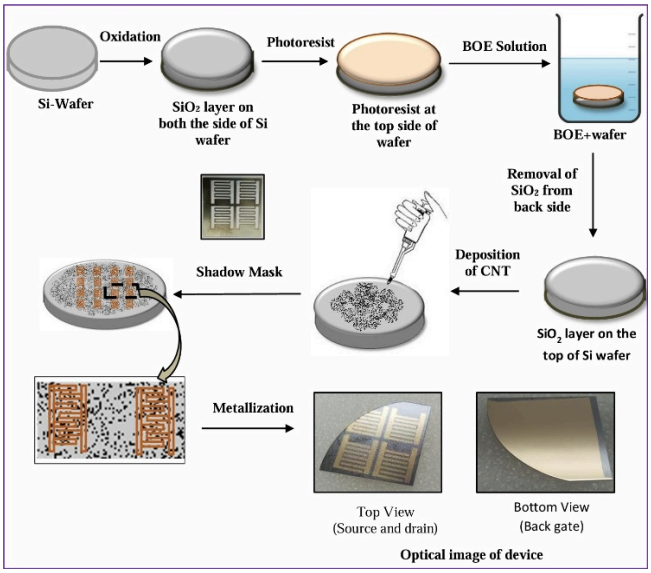

Figure 4. A sample step of CNTFET manufacturing [12]

3.2. Current obstacles

Despite the rapid progress in research in CNTFET, there are some obstacles that prevent the mass production of it.

3.2.1. Impurity

The impurity in CNT manufacture is a large factor in why CNT cannot achieve high-quality mass production. Even if a tiny fraction of the CNT is metallic, it would short the circuit and affect the on and off. The material standards for A-CNTs, set in 2024 by Yumeng Ze et al., are purity greater than 99.9999% ('six nines') [13]. Currently, the highest purity achieved is 99.99995%, higher than the requirement. However, this is only reported lab result, and the complicated processing steps make it far from achieving industrial mass production [3].

3.2.2. Cylinder shape

To control the variability of on current, there needs to be roughly the same number of nanotubes placed on each CNTFET device [14]. However, because of the cylindrical shape with a lot of surface area, the strong van der Waals intermolecular forces cause CNTs to stick together, making the uniform distribution hard to achieve [15].

4. Conclusion and future implication

Exhibiting different mechanisms of operation from traditional silicon MOSFETs, CNTFET has shown many benefits, including less short-channel effect, more carrier mobility, and lower power consumption. This reflects its great value for further studies. However, there are still many obstacles that prevent the industrial mass production of this technology. Namely, the impurity and problems caused by the CNTs' cylinder shape. If these challenges can be solved in the future, CNTFET would

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be a promising alternative to silicon MOSFET, solving the scaling issue while providing additional benefits.

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