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Temperature Dependence of CMOS

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Abstract. CMOS is the pillar of electronics industry due to its superiority such as low power consumption. However, its merits will not exist under inappropriate temperature ranges. This research aims to investigate the temperature-dependent characteristics of CMOS technology and how they affect the general performance of the intended applications such as wearable devices, image sensors, etc. This paper examines the temperature dependence of key CMOS characteristics, analyzing how changes in temperature affect parameters including power dissipation, noise immunity, etc. Using both literature review and TCAD simulation, the paper provides a comprehensive overview of the effects of temperature on CMOS performance. The findings underscore the critical need to consider temperature impacts in CMOS device operation, and suggest potential strategies for mitigating the adverse effects of temperature.

Keywords: CMOS, temperature-dependent, power dissipation, noise immunity, TCAD

1. Introduction

Complementary Metal Oxide Semiconductor (CMOS) technology is extensively employed in integrated circuits and related electronic products. The term “complementary” indicates that CMOS circuits incorporate both pMOSFETs and nMOSFETs. As predicted by Moore’s Law, the continuous downscaling of CMOS technology has led to faster device operation [1]. Currently, CMOS technology is widely applied in devices such as image sensors, owing to its high signal processing efficiency [2], and in medical diagnostic equipment, given its exceptional high-throughput capabilities [3]. However, when CMOS chips are exposed to overheated environments, such as within smartphones, or to extreme conditions like cryogenic temperatures in aerospace, their overall performance may degrade. Such malfunctions are highly undesirable for users, and there is a growing expectation for CMOS devices to operate reliably across a wider temperature range.

Numerous studies have explored the temperature dependence of CMOS devices, focusing on key parameters such as threshold voltage [4], drain leakage current [5], power dissipation [6], and transfer characteristics [7] across various thermal environments. Although these investigations have yielded crucial knowledge and greatly enhanced our grasp of the thermal impacts on CMOS efficiency, their scope regarding temperatures is frequently restricted. Numerous studies focus on a

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limited number of factors and usually examine these impacts within a specific range of temperatures.

To bridge the gaps in existing research, a more holistic analysis is warranted, one that synthesizes and integrates findings across multiple studies to provide a broader perspective on temperature dependence in CMOS technology. In pursuit of this objective, we have identified and selected several key parameters that are representative of CMOS performance under varying thermal conditions for further in-depth discussion and analysis. This comprehensive approach is expected to yield more robust conclusions, guiding the design and optimization of CMOS devices for operation in thermally challenging environments, with supplementary TCAD simulations primarily focusing on the relationship between temperature and threshold voltage.

This paper summarizes how specific CMOS parameters are influenced by temperature variations. First, a brief overview of the physics underlying CMOS technology including its structure and relevant principle is given in section 2. Section 3 focuses on four key parameters — power dissipation, switching speed, lifespan, and noise immunity—that represent the core advantages of CMOS technology. It is crucial to determine whether they can be strongly affected in various temperature conditions and that should be related to real applications. Additionally, in section 4, TCAD simulations conducted using Silvaco software imitate various thermal conditions and this will provide relatively substantial evidence for this review. Strategies on how to mitigate the adverse effects of temperature will then be discussed in section 5, and a few bottlenecks for current research on temperature dependence of CMOS will be presented. Finally, a comprehensive conclusion will be made on the basis of our research and it is hoped that possible mitigation strategies to be taken to respond to those negative effects of temperature.

Table 1 below briefly presents previous findings on various parameters.

Table 1. Previous findings on various parameters

Author(s)	Research Focus	Target Parameters	Key Reference
Kalara Shruti	Investigated the impact of temperature on CMOS circuit performance	Dynamic powerdissipation, switchingspeed, noise immunity	[4]
Rais K. F. , Balestra G.	Studied temperature dependence ofgate-induced drain leakage currentin silicon CMOS devices	Leakage current, gatevoltage	[5]
Clark William F.	Reviewed low-temperature CMOS technology	Leakage current, powerdissipation	[6]
Deen M. Jamal	Researched low-temperaturedependence of CMOS inverters	Voltage transfercharacteristics	[7]
Smith M. T. , Tupper D.	Studied the impact of temperatureon CMOS circuits	Power dissipation, lifespan, thermal runaway	[23]

2. Physics of CMOS

Complementary Metal-Oxide-Semiconductor (CMOS) technology is built upon two types of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs): PMOS and NMOS. Both types share

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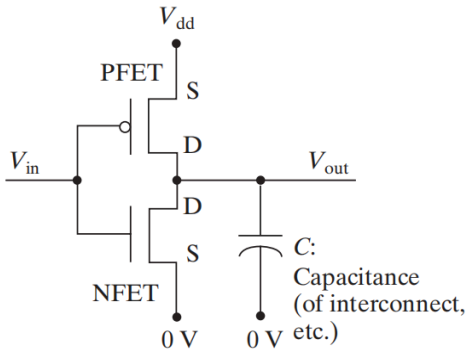
similar structures and operating principles, differing primarily in the use of P-type and N-type semiconductors. For simplicity, NMOS is taken as example for explanation. NMOS transistors use P-type semiconductor as its body, with three terminals on the body: “source” and “drain” terminals on the two sides, and “gate” terminal in the middle but disconnected to the body [8]. For NMOS, source and drain areas are made of N-type semiconductor. The gate is made of metal, separated from the body by insulative material, usually oxide, to allow electric field effect to happen. When a positive voltage exceeding the threshold voltage is applied to the gate, an N-type channel forms beneath the gate on the semiconductor surface, allowing current to flow between the source and drain. This mechanism allows NMOS to be used as electronic switch. It is important to note that NMOS conducts when positive threshold voltage is applied, while PMOS conducts when negative threshold voltage is applied. This complementary behavior is fundamental to the operation of CMOS technology.

In CMOS, an input signal is transmitted to both the gates of NMOS and PMOS, as is shown in Figure 1. The source of PMOS is connected to Vdd, the main power voltage that represents logic level 1, while that of NMOS is connected to the ground that represents logic level 0. Their drains are both connected to the output. These two MOSFETs operate in a push-pull manner, which means when one transistor is turned on, the other transistor must be off, due to the complementary relation, to achieve logic inversion. When input voltage is logic level 0, PMOS conducts while NMOS is off, so logic level 1 is connected to the output. This architecture allows CMOS circuits to maintain extremely low power consumption in a static state because when the input signal is stable, one of the two MOSFETs is always in the off state, thereby blocking the DC path from the power supply to ground.

CMOS technology is distinguished by several key features. Firstly, its low power consumption [9-11] is particularly advantageous in portable and battery-powered devices. The second feature of CMOS is its high noise margin [12]. Since they rely on potential difference rather than current to operate, they have strong resistance to noise. Moreover, the features of CMOS also include high integration, the ability to integrate a large number of transistors on a small chip area, and good logic swing due to the output level of CMOS circuits being close to the power supply voltage and ground potential.



(a) Basic circuit notation of CMOS inverter

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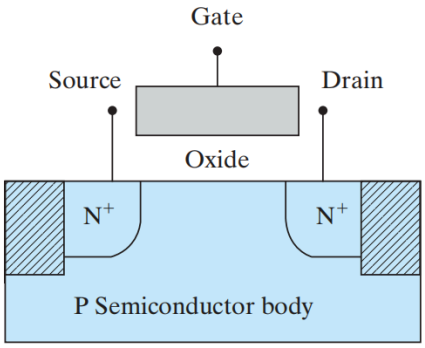

(b) Basic structure of NMOS

Figure 1. Primary view of CMOS in the level of circuit and device

3. Temperature dependent parameters

3.1. Power dissipation

The main components of CMOS power dissipation are dynamic and static power dissipation. Dynamic power dissipation happens when CMOS is switching, while “static” means that it happens even when there is no changes made to the CMOS. The cause of static power dissipation can be further divided into subthreshold current and reverse-bias leakage current. Temperature has direct effect on reverse-bias leakage current, while threshold voltage of CMOS is the medium through which temperature affects the power dissipation of CMOS and subthreshold voltage.

3.1.1. Reverse-bias leakage current

Reverse-bias leakage current is due to the constant potential difference when one transistor is on and the other is off. For example, when input is 1, the output node, which is connected to the drain of PMOS, is 0, while the source of PMOS is connected to Vdd. This generates reverse saturation current in the diode existing in the PMOS, causing power loss. The expression of this reverse-bias leakage current is given by formula (Eq.1) [13],

$$I_{reverse} = AJ_s\left(e^{\frac{qV_{bias}}{kT}} - 1\right) \tag{1}$$

where A is the area of drain diffusion and Js is the leakage current density. Because Js nearly doubles for every 9 degree Celsius increase in temperature [14], increasing temperature will increase the power consumption due to this reverse-bias leakage current.

3.1.2. Temperature and threshold voltage

The relation between temperature and threshold voltage is clarified in this section before going to the parts for subthreshold current and dynamic power dissipation.

When temperature increases, the threshold voltages of NMOS and PMOS both show a decreasing trend, according to the graph below in Figure 2(a) [15].

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Furthermore, the change in threshold voltages, due to variation in temperature, will have an different effects on dynamic and static power dissipation. Increasing threshold voltage, for example, will decrease the subthreshold current, while increase the dynamic power dissipation if delay problem is not intended to be severer.

3.1.3. Subthreshold current

Subthreshold current exists due to carrier diffusion between source and drain, when Vgs has exceeded a weak inversion point but still below threshold voltage [16]. When temperature increases, threshold voltage decreases and subthreshold current increases exponentially, presented by the graph below in Figure 2(b) [16].

3.1.4. Dynamic power dissipation

Dynamic power dissipation happens only when switching. For example, when input logic level changes from 1 to 0, the output logic level will change from 0 to 1. In the switching process, the power supply generates current to charge the load capacitance at the output node, in order to change the output node voltage to 1. These current flows both through the PMOS and load capacitance, so half of the power drawn from Vdd, which is equal to $\frac{1}{2}C_LV_{dd}^2$, is dissipated in the PMOS, which acts like a resistor in simple RC circuit. Similarly, the same amount of power is also dissipated in NMOS when the opposite transition is being done, when load capacitance is discharging through the NMOS to the ground. In total, the power dissipated in one switching cycle, from 0 to 1 then back to 0, or the opposite, is $C_LV_{dd}^2$. Then if taking into account the clock frequency that the CMOS is operating and the average number of switching cycle that CMOS does in one clock cycle (node transition activity factor), the equation for dynamic power consumption can be shown as formula (Eq.2) [14],

$$P_{switching} = a_{0->1}C_LV_{dd}^2f_{clk} \tag{2}$$

where $a_{0->1}$ is the node transition activity factor, C_L is the load capacitance and f_{clk} is the clock frequency. It is clear from the above expression that there is a quadratic relation between $P_{switching}$ and Vdd, so for the sake of lowest dynamic power dissipation, Vdd should be set as low as possible. However, in practice, the decrease in Vdd will adversely affect the speed that CMOS corresponds to changes in input, according to the graph below in Figure 2(c). The graph shows that as Vdd (supply voltage) decreases and approaches the threshold voltage, delay time increases, and the slope of the graph becomes steeper, which means delay time increases even more rapidly. Since decreasing Vdd, which helps keep the dynamic power low, will also severe the delay problem, a measure to take is choosing CMOS with threshold voltage as low as possible, so that Vdd can be set lower to decrease dynamic power dissipation. However, if temperature is too low and the designer does not want to sacrifice the working speed of CMOS, the Vdd will need to be set high, which increases dynamic power dissipation.

To conclude the effect of temperature described above shortly, temperature influences the dynamic power and subthreshold current power of CMOS by affecting its threshold voltage, and it also has direct effect on the reverse-bias leakage current power. In order to decrease the overall power consumption, the temperature should not be too high, which increases the static power

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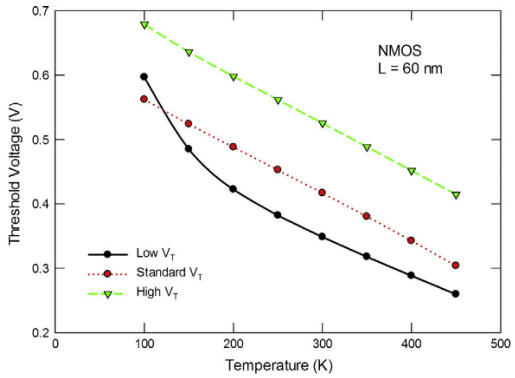
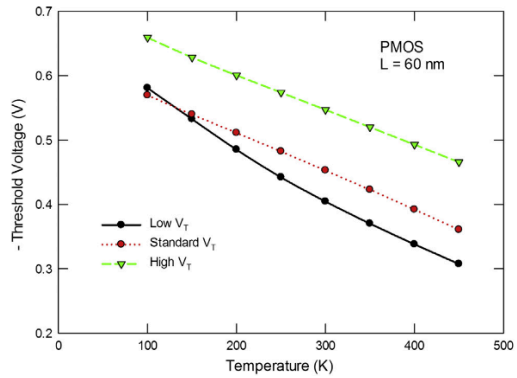
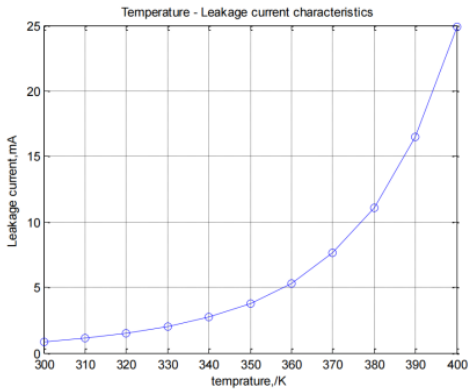
dissipation, and not too low, which will increase the dynamic power dissipation if not severing the delay time.



(a) Relationship between threshold voltage and temperature in NMOS



(b) Relationship between threshold voltage and temperature in PMOS



(c) Relationship between leakage current and temperature

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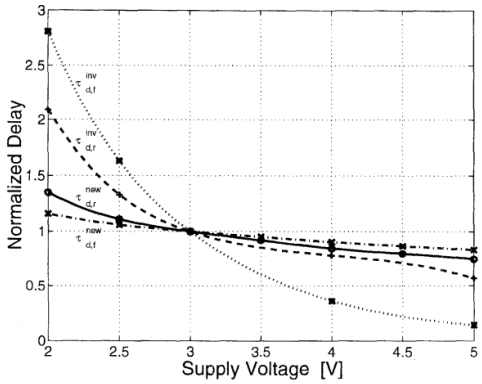

(d) Relationship between normalized delay and supply voltage

Figure 2. Research results of electrical behaviors [13, 15]

3.2. Switching speed

The threshold voltage of MOSFET is an important parameter that determines it's on and off states. As the temperature increases, the threshold voltage of MOSFET usually decreases. This means that under the same input voltage, MOSFETs are more likely to turn on at high temperatures, but this may also lead to instability and increased noise during the switching process. However, it should be noted that some specific designed CMOS circuits may use temperature compensation mechanisms [17-19] to reduce the impact of threshold voltage changes with temperature on switching speed.

3.2.1. Carrier mobility analysis

Carrier mobility refers to the speed at which charge carriers move in a semiconductor. As the temperature increases, the carrier mobility usually decreases. This will slow down the signal transmission speed in CMOS circuits, thereby affecting the switching speed. The decrease in carrier mobility can also affect the performance parameters of devices such as CMOS image sensors, such as conversion gain and saturation output. In high-temperature environments, the power consumption of CMOS circuits may increase because the decrease in carrier mobility requires higher voltage or current to drive the circuit. Meanwhile, high temperatures can also lead to heat accumulation inside CMOS chips, further affecting switching speed and circuit stability. Therefore, when using CMOS devices in high-temperature environments, appropriate heat dissipation measures need to be taken to maintain the chip temperature within a reasonable range.

3.2.2. Performance at higher temperature

Research has shown that the switching speed of CMOS logic cells significantly slows down with increasing temperature within the temperature range of 25-250℃. For example, some experimental results show that the switching speed of CMOS logic cells may be 65% slower at 250℃ than at room temperature [20-22]. Other studies have analyzed the performance changes of CMOS circuits at different temperatures through simulation, including the variation of threshold voltage, carrier mobility and other parameters with temperature. In summary, temperature has a significant impact on the switching speed of CMOS. In high-temperature environments, the switching speed of CMOS circuits may slow down due to factors such as a decrease in threshold voltage, a decrease in carrier mobility, and an increase in power consumption. Therefore, when designing and using CMOS

DOI: 10.54254/2755-2721/2025.29821

devices, it is necessary to fully consider the influence of temperature factors and take corresponding measures to maintain the stability and performance of the circuit.

3.3. Life span

According to Smith's research [23], CMOS devices generate heat during operation and the increase in temperature will affect the performance and life of the device. Thermal runaway is one of the failure modes to CMOS. Thermal runaway occurs when an exothermic reaction goes out of control, that is the reaction rate increases due to an increase in temperature causing a further increase in temperature and hence a further increase in the reaction rate, which may cause some effects to the life of CMOS. There are some possible reasons for the temperature to have impact on the life of CMOS.

3.3.1. CMOS gate oxide layer failure

At high temperatures, the gate oxide is easily damaged, resulting in an increase in leakage current, which in turn shortens the device life. The leakage current is increased, and the device life is shortened [24]. Increased temperature can lead to reduced carrier mobility, affecting the performance and response speed of the device.

3.3.2. Thermal runaway

Thermal runaway may occur in devices at high temperatures affecting the stability of the entire circuit negative effects accumulate. Long-term high temperature operation will lead to the accumulation of negative effects in the device and accelerate the aging of the device. Optimized heat dissipation design can effectively reduce the operating temperature of the device and extend the life of the device. It effectively reduces the stress of CMOS while it is working and can provide a longer time before the temperature increases.

3.3.3. Temperature monitoring

For maintaining the dependability and durability of CMOS gadgets, it's crucial to adopt instantaneous surveillance of their operational thermal state. Through consistent monitoring of heat fluctuations, swift and efficient measures can be implemented to reduce the likelihood of extreme temperature increases, which can negatively affect the functioning of devices and possibly cause irreversible harm [25]. Intervention strategies could involve the activation of cooling systems or the dynamic modification of the device's operational capacity to diminish heat output.

Additionally, improving the CMOS production process is crucial in boosting the device's heat resistance. Accomplishing this involves fine-tuning both material choosing and production methods, with the goal of enhancing the device's resilience to elevated temperatures [26,27]. Progress in these techniques preserves the structural soundness of CMOS devices in high temperature scenarios, which guarantees steady performance and extends their operational lifespan. These improvements could include incorporating materials known for their higher thermal conductivity, refining deposition techniques, and crafting durable structural designs that withstand high-temperature settings without deterioration.

Currently, the accurate research in life span is mainly constrained to 22-nanometer node or above due to challenges in both the fabrication process and the characterization techniques at smaller nodes. One research group suggests that using high-k materials for oxide layer and applying

DOI: 10.54254/2755-2721/2025.29821

machine learning framework can predict the overall durability and quality for CMOS in smaller scales [28]. However, this is also restricted to room temperature. For a wider thermal range, more research needs to be further carried out.

3.4. Noise immunity

In electronic devices, noise often appeared as an unpleasant aspect. Frequently, noise can lead to errors in transmitting data, lower signal-to-noise ratios, and ultimately cause a circuit's malfunction. Also, the interfere of noise will make the signal become less likely to be predicted or analyzed. For instance, in Figure 3, $x_1(t)$ is a sinusoidal signal, while $x_2(t)$ is a signal with noise, and $t_1$and t_2 are two specific moments. The value at t_1 can be predicted with the data of the previous signal, but the value at t_2 is uncertain due to its randomness. CMOS circuits, however, are more resistant to noise in a certain level, mainly due to two reasons. Firstly, for CMOS circuit's dynamic conditions, as it is discussed in 3.1, power consumption mainly occurs in switching process. This suggests that the undulation from power will have little impact on the whole circuit's noise. Secondly, in common CMOS circuits, differential pairs and signals are used to diminish the common-mode noise. By replacing an original signal with two of equal amount and opposite phases, their difference will remain the same with the expected output signal, and there will be no noises. In normal conditions, the feature of the noise immunity is a superiority of CMOS. But a few researches suggest that temperature serves as a key environmental factor influencing the intensity of noise within CMOS circuits. Basically, there are two dominant types of noises in CMOS circuit that are temperature-dependent, thermal and flicker noise.

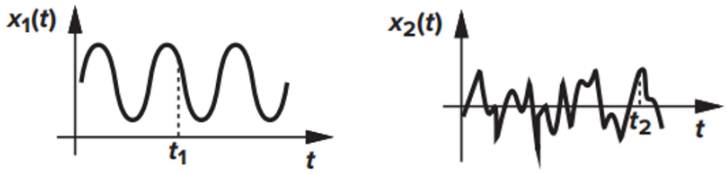

Figure 3. Signal without noise (left) and with noise (right) [1]

3.4.1. Thermal noise

Thermal noise mainly occurs in resistive components. It is caused by the random motion of charge carriers within a conductor and is exactly proportional to temperature. Regardless of the frequency component, the relationship between noise power density $S_{thermal,v}$ (in voltage) or $S_{thermal,i}$ (in current) and temperature T can be shown as the formula (Eq.3 & Eq.4) below,

$$S_{thermal,v} = 4kTR \tag{3}$$

$$S_{thermal,i} = 4kT/R \tag{4}$$

where k is Boltzmann's constant and R is the resistance [29].

There is a clear conclusion that for a certain device, its thermal noise will increase as temperature rises assuming that its resistance is constant, and thermal noise may not be the top concern in cryogenic environments. Nevertheless, throughout the experimental work conducted by Tedja et al. [30], which was based on a one-dimensional charge-sheet model and had taken all inversion regions

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in the saturation region into account, body effects of a MOSFET may also affect the thermal noise. For this one-dimensional model, noise expression can be derived from the carrier transport process of drift or diffusion, and it can be used to describe the noise behavior of different inversion regions. Therefore, the equation for current can be presented as formula (Eq.5),

$$S_{thermal,\,i} = 4kT\gamma g \tag{5}$$

where γ is the noise coefficient and g is the channel conductance at V_{DS}= 0.

Currently, thermal noise is measured by attaching a resistor to an oscilloscope while applying a few models. Scholten et al. [31] propose an improved series of models for measurements in deep-submicron CMOS. By utilizing a condensed MOS model focused on surface potential to more accurately represent carrier mobility and velocity saturation, a more detailed characterization of each experimental result can be better presented while the necessity for carrier heating influences or additional variables may also be eliminated.

3.4.2. Flicker noise

Flicker noise, or 1/f noise, is notably distinct at lower frequency ranges, correlating with the entrapment and imperfections at the interface between oxide and semiconductors in MOS transistors. Thus, its noise power density is affected by a few more parameters, as the equation (Eq.6) shown below(in current) [29],

$$S_{thermal,\,i} = \frac{KF \cdot W}{fL^2 C_{OX}} \left(\frac{I_{ds}}{W}\right)^{AF} \cdot kT \tag{6}$$

where KF is proportional to the oxide trap density, AF is depended on Coulombic scattering, f is the frequency and W, L, C_{ox}, are respectively the width, length and the per-area oxide capacitance of the MOSFET.

The 1/f noise arouses for varied reasons in two type of MOS. An experiment carried out by Chang et al. [32] suggested that the 1/f noise in devices of n-channel type primarily stems from changes in carrier density, whereas in those of p-channel type, it predominantly stems from fluctuations in mobility.

On the other hand, 1/f noise mainly depends on frequency, instead of temperature, and it is far lower than thermal noise. In conditions with frequency of 100 MHz or above, 1/f noise can be neglected.

In addition to thermal and flicker noise, some other noises also exist. Shot noise, which is relatively more common in diodes, refers to the random fluctuation caused by the dispersion of electrons in the electron stream [33]. The essence of its temperature dependence is actually caused by the velocity of carriers. Subthreshold noise, similarly, is influenced by temperature due to the thermal activation of carriers and this kind of noise is often more significant in deeply scaled devices. However, it is thermal noise that is overall the most prominent noise in CMOS circuits when it comes to temperature dependence. To promise a better performance of electrical devices, we suggest that they should not be used in extremely heated situations, or simply apply a cool-down system to them in order to guarantee the accurate transmission of signals.

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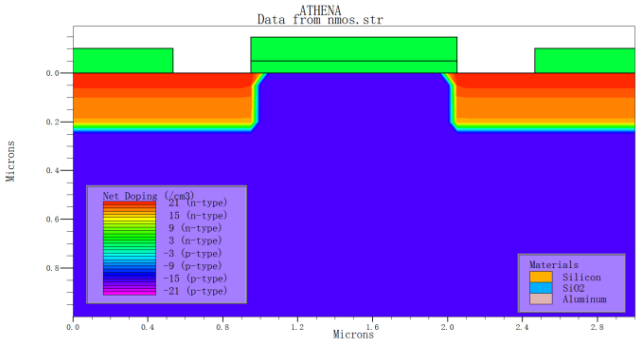
4. TCAD analysis

In this section, we conducted a series of simulation on the relationship between threshold voltage and temperature to verify how power dissipation is dependent on temperature. It is worth noting that in this simulation, we ignore the secondary effects, especially for the subthreshold voltage.

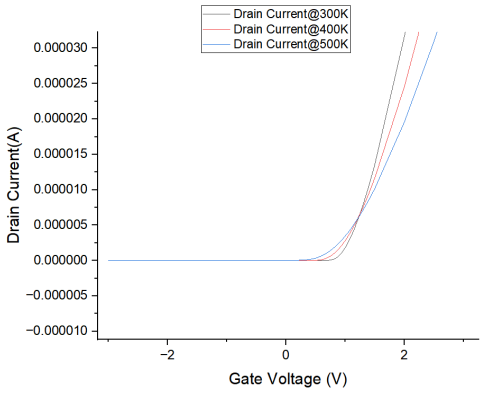
To simplify the analysis, we use NMOS for simulation. The applied material and parameter of NMOS are depicted in Table 2.

Table 2. Material and parameter of NMOS

Gate oxide layer	SiO_2
Main body	Silicon
Electrode	Aluminium
Doping	Phosphorous
Doping concentration	$1x10^{20}cm^{-3}$for each n-well (Figure 4(a))
Channel length	1.0 μm
Calculation method	Newton Iteration
Simulation Model	Shockley-Read-Hall [34]



(a) Structure of NMOS built for calculation



(b) Threshold voltage@300, 400, 500K

Figure 4. Structure in simulation and results of threshold voltage under various temperatures

Figure 4(b) illustrates that in the range from 300K to 500K, the threshold voltage will decrease from 0.7V to 0.2V, which is the similar conclusion with that of Figure 2(a). This indicates that as

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temperature arises, the device will switch on at a rather low voltage. Although it may enable the device to work with lower power supply, the static power dissipation will increase due to the increase in drain current. It is also found out that as temperature gets higher, the subthreshold effect becomes obvious, which leads to an extra increase in power dissipation and shortens the lifespan of the device.

Designers typically need to find an appropriate threshold voltage based on the application scenario in order to achieve the best balance between performance and power dissipation, with the additional consideration of the operating temperature of certain devices.

5. Discussion

Apart from the effect of working environment, the main reason of variation of operating temperature is the heat generated by CMOS itself, which takes time to dissipate to the surrounding to return to its original temperature. Hence, the main task is to increase the rate at which extra heat energy is dissipated to the surrounding, in order to maintain a reasonably stable temperature. In this section, three possible measures are provided for this purpose: PCB trace with lower thermal resistance, heat sink and heat pipe.

5.1. PCB trace with lower thermal resistance

PCB traces act as the “wires” connecting different components and voltage supply on PCB, so they are throughout the PCB. The trace can be utilized for better heat dissipation by using material of lower thermal resistance, which is defined as the ratio of temperature difference between two faces of a material to the rate of heat flow per unit area, for the material of it. The lower is the thermal resistance, the higher is the heat loss rate of material [35]. These traces can also help distribute heat more evenly throughout the PCB, hence preventing overheat of a certain area on PCB. However, it means that the component with higher heat dissipation will affect other components on PCB, which should be considered by the designer.

5.2. Heat sink

Heat sink is essentially a metal structure that is directly attached to the semiconductor component. The purpose of it is to provide a low thermal resistance path to allow heat going from the heat source and the ambient, by means of convection and radiation. Because the efficiency of heat sink is directly related to the surface area, finned designs are usually applied for the geometry of heat sink [36].

5.3. Heat pipe

The graph in Figure 5(b) illustrates the structure and principle of heat pipe. A heat pipe consists of metal envelope, wick and a chosen kind of fluid. The metal envelope is the exterior of heat pipe, with wick, a microporous structure of metal, on its inner surface. The fluid, which can absorb, carry and release the heat, is located in the space inside the wick. The whole heat pipe is divided into three parts: evaporator, adiabatic section and condenser. The heat from component will evaporate the fluid into vapor. The pressure difference due to different temperature will drive this vapor from evaporator to condenser, where the vapor will release the latent heat of vaporization to the heat sink, becoming fluid again [37]. The fluid needs to be chosen carefully to allow vaporization and condensation to happen due to heat from the components.

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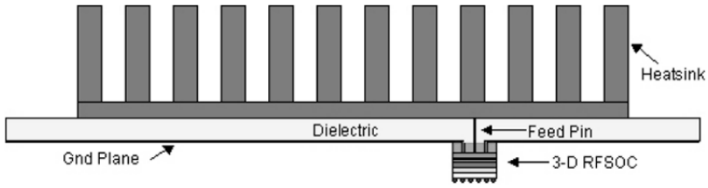
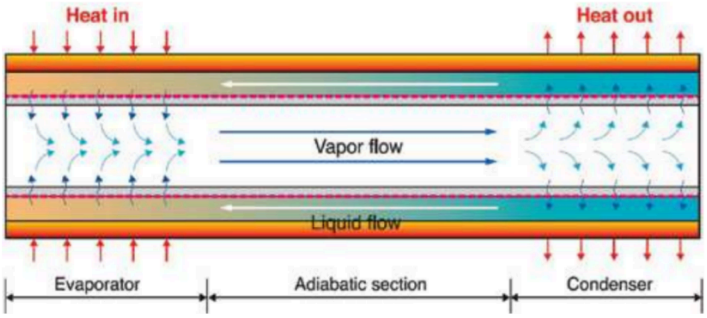


(a) Structure of heat sink [38]



(b) Structure of heat pipe [37]

Figure 5. Two devices to maintain temperature

6. Conclusion

The study thoroughly examined the temperature reliance of different CMOS parameters, illuminating the way fluctuations in temperature can greatly affect the efficiency and dependability of devices based on CMOS. Utilizing a blend of literature analysis and TCAD simulations, this study delves into key elements like power dissipation, switching speed, longevity, and resistance to noise in CMOS circuits, offering crucial understanding of the difficulties and possible methods to mitigate thermal effects.

With the escalation of temperature, vital variables like threshold voltage, carrier flexibility, and leakage current experience substantial alterations. These changes can lead to higher energy dissipation, reduced switching speed, and potentially weakened noise immunity. In particular, a drop in threshold voltage correlating with an increase in temperature typically elevates the subthreshold current, whereas diminished carrier mobility impedes signal transmission, impacting the aggregate speed of the circuit. Also, the intensity of thermal noise escalates at increased temperatures, potentially further undermining the signal integrity within CMOS circuits.

Furthermore, this research highlights the importance of taking into account these thermal impacts in the planning stage of CMOS-oriented applications. In cases like wearable tech and aerospace electronics, where operational temperatures differ greatly, adopting design approaches to counteract the detrimental impact of temperature changes is vital. This process may include choosing materials superior in thermal characteristics, crafting circuits equipped with temperature balancing features, or using sophisticated cooling techniques to maintain consistent functioning. Furthermore, as discussed in Section 5, integrating heat pipes and heat sinks to enhance heat dissipation can effectively mitigate the negative impact of temperature. As CMOS technology continues to evolve, it is essential to address its temperature sensitivity to optimize the performance of CMOS-based applications across diverse sectors.

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