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The Hardware Implementation of Digital Filter Algorithms for Headphone Noise Cancellation

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Abstract. Driven by ongoing innovation in consumer electronics, today's headphones embody the convergence of acoustics, digital signal algorithms, and integrated circuitry, moving far beyond the concept of a conventional audio device. In active noise cancellation (ANC) applications, digital filters play a central role. The degree of coordination between algorithm design and hardware implementation directly affects the system's ability to suppress noise, manage power efficiently, and reduce production costs—all of which determine a product's competitiveness in the marketplace. This research focuses on the two primary digital filter structures—Finite Impulse Response (FIR) and Infinite Impulse Response (IIR)—in conjunction with adaptive algorithms such as the Normalized Least Mean Squares (NLMS) and simplified LMS variants. A detailed analysis is conducted on their implementation and optimization strategies from a hardware perspective. The study builds a complete analytical framework that traces the path from algorithm logic to module mapping and finally to hardware realization, enabling systematic evaluation of design efficiency. Moreover, a four-dimensional evaluation model is developed to compare design solutions across noise reduction capability, silicon area, power consumption, and cost efficiency. The analysis reveals that the FIR-NLMS combination, thanks to its linear phase property and strong cancellation precision, is more suitable for high-end headphone systems. Conversely, the IIR filter paired with a simplified LMS algorithm offers better performance for cost-sensitive applications due to its recursive structure and efficient hardware utilization. Guided by real product demands, this paper outlines a balanced design strategy that integrates performance, cost, and energy efficiency, providing practical guidance for future digital filter hardware design in ANC systems.

Keywords: digital filters, active noise cancellation, hardware implementation

1. Introduction

Nowadays, headphones have transformed from basic audio playback tools into sophisticated intelligent devices that combine acoustic engineering, signal processing, and integrated circuit technologies [1,2]. In active noise cancellation systems, digital filters serve as a core element, where the alignment between algorithmic design and hardware realization critically influences the headphones' noise reduction performance, power efficiency, and manufacturing cost—factors that collectively define the market competitiveness of modern audio equipment [3].

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Headphones have evolved, in recent years, from a simple means of delivering audio signals to its listeners into truly intelligent products, which involve acoustic, signal, and integrated-circuit engineering [1,2].As a fundamental component, digital filters is considered in many active noise cancellation designs, where algorithm design and hardware implementations have a direct impact on the noise canceling efficacy, the power consumption and manufacturing expenses of these headphones–metrics that are jointly assessed for the commercial viability of current audio devices [3].

The central idea of active noise cancelling technology is the destruction interference of the sound waves: recording of the environmental noise by a microphone and simultaneously synthesizing the anti phase signal by digital filter instantaneously and delivering it by a speaker. and further mixing it with the original noise for the cancellation purpose. Current day, mainstream of the digital filtering methods are mainly in two forms FIR or IIR with hardware implementation point of view [4]. Because of their linear phase characteristics, the FIR filter provides very good audio quality. However, its feedforward configuration requires a large number of multipliers and delays, resulting in a larger implementation area. IIR filters adopt a recursive approach that can decrease area overhead and enhance power efficiency, but suffer from nonlinear phase characteristic that can degrade cancellation accuracy [5]. To achieve the appropriate trade-off between performance and resource usage, in most cases, adaptive algorithms like LMS and NLMS are used [6,7]. Because in their implementation, they have to adaptively update the filter coefficients such that the quality of noise suppression remains robust to variations in the acoustic environment, consequently adding a higher burden to the hardware's online processing capabilities.

For digital filter circuits designed by today's consumer electronics industry, different constraints might be set. To address such constraints, a filter circuit designer needs to confront some fundamental issues: for different product positioning, choose different algorithms and hardware architectures accordingly; for several priority lists such as noise suppressing performance, latency, power performance, and cost performance, we need to make a trade-off among them. A comprehensive review on various filter algorithms hardware implementation strategies— and a comparison on their performance properties and application— is very important to the maturity development of noise reduction technology [8,9].

Although there are many research studies in hardware implementation of digital earphone noise canceling filters, there are still scopes and open areas in this field. First, most of the previous works, focuses on optimization of an individual method i.e. using minimize the power consumption in the design of FIR structure or to improve the noise cancellation accuracy in the design of IIR and then without providing an analysis to show a clear distinction between the two major structures (i.e. FIR using NLMS or IIR using Simplified LMS. Moreover, due to its absence of system-level comparison, this disallows those who study the material to have a clear sight on adapting the solutions to each hardware limitation respectively. Second, the evaluation performances presented in the literature do not always stay within the performances that have real application in manufacturing. Each solution is typically introduced at a unique production and energy cost. Existing research does not connect the performances to the headphone product positioning in the market. As a consequence, this misalignment causes inefficient device engineering, by including costly high-end filter configurations in devices considered of low cost, or opting for basic solutions to improve audio playback in high-end devices [10-12].

In comparison with the aforementioned works, this paper has the following advantages, which could be considered as special characteristics of this work. On the one hand, as a methodological aspect, it proposes the fusion of the hardware architecture of the two basic techniques within an

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unified analytical scheme in form of "logical architecture–module mapping–hardware implementation and optimization–multidimensional performance analysis" thus making clear the mapping between individual hardware components and algorithm steps. Second, on data representation, it proposes a four-dimensional comparison framework of "noise reduction capacity–chip size– power dissipation– price" so as to quantitatively compare the performance of FIR and IIR schemes. Third, in a practical application aspect, based on real-world headphone product requirements, the paper develops guidelines for decisions from cost and power-efficiency perspectives and gives hints for potential direction to the future hardware optimization of digital filters in ANC headphone products, making the results academic as well as engineering value.

2. Disassembly and analysis of hardware implementation

2.1. Hardware implementation of IIR filters using the adaptive simplified LMS algorithm

The combined implementation of IIR filters and adaptive simplified LMS algorithm is the optimal technical route to consumer noise canceling headphones for beginner markets. This is because two improvements compatible with low cost and low power consumption, a basic recursive design that reduces number of hardware components, and algorithm simplification that reduces superfluous calculations [13]. This paper will gradually analysis the scheme by a bottom-up way in the following sections: according to the logical diagram of the signal flow, mapping the algorithm steps to the hardware modules and finally introducing the implementation methods and the optimization to improve the performance.

The logical structure of the IIR solution is shown below as Figure 1. Ambient noise x(n), which is collected from the side of the headphones, is passed to the IIR adaptive filter to produce a canceling signal y(n). y(n) is added back to cancel with the ambient noise signal d(n) at the surroundings of the speaker, collected from the feedback microphone. The produced residual signal e(n) will be output to the LMS adaptive algorithm for LMS computation. After simplification of the LMS adaptive algorithm, the new adjustment coefficient are calculated according to the e(n) signal to better make the filtering and noise reduction performance of the IIR adaptive filter, which is an infinite iteration as the core logic of IIR solution, so that y(n) approaches d(n) infinitely to achieve the purpose that error e(n) tends to zero, and thus achieves better and better noise reduction performance [13-15].

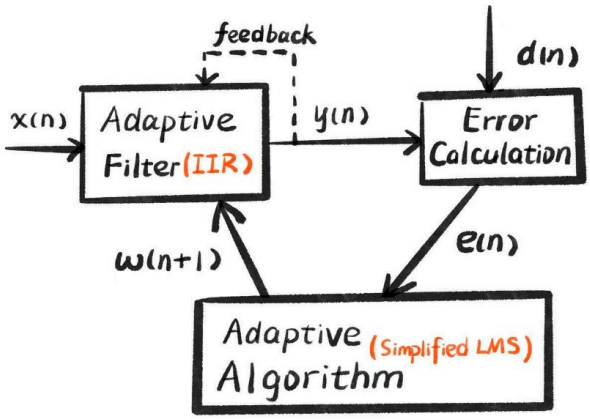

Figure 1. Basic logical framework of the IIR+ Simplified LMS scheme

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According to the above logic structure, we can distinguish the four modules that are implemented in hardware for the IIR scheme: IIR recursive filtering module, error calculation module, simplified LMS algorithm module, coefficient storage and synchronization module. In fact, the last module is not the highlight part of the algorithm and we will not describe it here. Next, we study the hardware design and implementation of the first three modules in order.

At the heart of the IIR recursive filtering module lies the differential equation for a 4th-order IIR filter, expressed as [5]:

$$y(n) = \sum a_i \cdot x(n-i) + \sum b_j \cdot y(n-j) \tag{1}$$

Where "a_i" denotes the feedforward coefficient and "b_j" denotes the feedback coefficient. Theoretically, the output of an IIR filter depends on both the current and past input signals, as well as past output signals. Therefore, a bidirectional delay chain is frequently employed to dynamically store four stages of data—typically constructed from flip-flops or register arrays to meet the timing requirements of the sampling rate. Most studies in filter implementation reduce the number of multiplier units by sharing resources between registers and multipliers [15]. To further conserve resources, the module implements multiplier multiplexing through clock-gating technology [13,15]. The first half of the clock cycle processes the feedforward multiplication, while the second half handles the feedback multiplication [6].

The y(n) signal output from the IIR module is transmitted to the next module for error calculation. The core calculation of the error calculation module focuses on a simplified design, with the equation as follows [5]:

$$e(n) = d(n) - y(n) \tag{2}$$

A 10-bit ADC is used to acquire the environmental noise signal d(n). A 16-bit subtractor performs the operation d(n) - y(n), outputting the error signal e(n). To mitigate interference from y(n-j) on input d(n) in the feedback path (e.g., electromagnetic coupling), a 1ns delay unit is serially inserted in the feedback signal transmission path. This temporally decouples y(n-j) from d(n), trading an acceptable minor time deviation for signal purity [4,5].

After calculating the error signal e(n), the signal is transmitted to the LMS module for optimization computation. The coefficient update module constitutes the core of the LMS plan, with its formula simplified to [5,6]:

$$w(n+1) = w(n) + \mu\, e(n)\, x_{adjust}(n) \tag{3}$$

The new coefficient w(n+1) replaces the previous old coefficient w (n). The fixed step factor μ. Use 16 bit multiplier to do multiplication. The simplified LMS because of having fixed step size factor , with huge external noise it may fluctuate too much, due to this the value e(n) may change significantly, due to these changes w(n+1) may oscillate significantly or at worst we may get multiplication overflow. Thus, the cancellation output by the speaker might be inaccurately aligned to cover the original noise, which would lead to audible errors. To reduce this drawback, generally an input power calculating module is applied to help the principal algorithm module.

The input power calculation module employs periodic power computation [6].

$$P_{avg} = \frac{1}{N} \sum_{k=0}^{N-1} x^2(n-k) \tag{4}$$

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Every 10 ms, calculations are performed on 480 input samples (at a 48kHz sampling rate) using multipliers, accumulators, and dividers. The hardware incorporates two comparators, $P_{high\ threshold}$ and $P_{low\ threshold}$. Based on these comparisons, different gain scaling factors G are output. Finally, x(n) is multiplied by G via the multiplier, yielding the adjusted signal $x_{adjust}(n)$. Additionally, w(n+1) and w(n) will be blended using a 1:3 weighting: w(new)=0.25×w(n+1)+0.75×w(n). This secondary blending reduces coefficient fluctuation. These two optimization methods execute sequentially, limiting coefficient change rates to ≤5% [4].

The calculated result w(n+1) in the LMS module is then input to the IIR filter module to serve as the new feedforward coefficient "a_i" for minimizing the difference equation with improved overall noise attenuation performance for the headset. This constitutes one round iteration of the IIR realization through hardware implementation and algorithm decomposition.

2.2. Hardware implementation of FIR filters using the adaptive NLMS algorithm

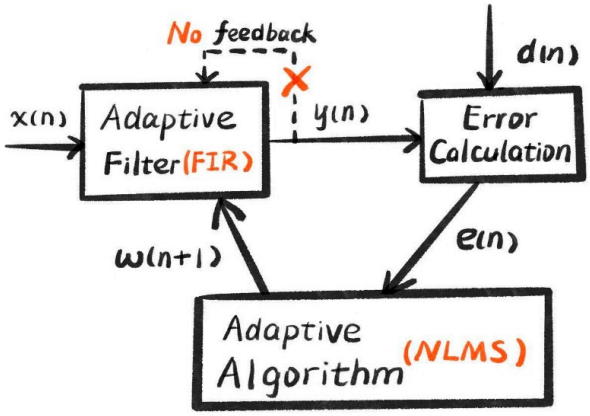

Figure 2. Basic logical framework of the FIR+NLMS scheme

The combination of FIR filters and the adaptive NLMS algorithm is the foundational method for premium noise-canceling headphones to achieve highly accurate noise suppression. This system's hardware design is built upon the operational principle of "fixed FIR filtering combined with dynamic NLMS coefficient updating" [4,14].

Surprisingly, the high-level architecture of the FIR-based solution is in principal similar to the one of the IIR solution, with four units forming the overall structure: an unit for the FIR filter, an error generation unit, an updated coefficients calculating unit, and a unit for updating the NLMS coefficients memory [4].The rest of this work will explore in depth the main differences between design choices and hardware implementation of FIR and IIR which show the unique advantages of the implementation, module by module of FIR.

Distinct from the feedback-driven structure of IIR filters, the FIR filter's principal module adopts a tapped-delay line structure, which directly aligns with the linear convolution process inherent to the FIR algorithm [7,14].

$$y(n) = \sum_{k=0}^{N-1} h(k) \bullet x(n-k) \tag{5}$$

Specifically, the output signal y(n) is determined by a combination of feedforward input signals x(n-k), which are delayed by k time units, and the fixed unit impulse response coefficients h(k), as

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dictated by the filter's design goals. This clearly illustrates the “non-feedback” nature of FIR, meaning the output depends only on past input values, rather than on previous output values, as is the case with IIR filters. As a result, hardware realization only requires a feedforward delay structure, making it simpler to guarantee system stability [14]. For this application, D-type flip-flops are utilized as delay components. To meet the 20 Hz to 20 kHz audio bandwidth requirement for headphone noise cancellation, a delay chain with 8 to 16 stages is implemented. A 16th-order FIR filter requires exactly 16 delay units. The 16–24-bit fixed-point multipliers used meet high-fidelity audio processing needs. Adders have 4–6 more bits than multipliers, and this redundancy prevents overflow when accumulating intermediate signals.

The error calculation module serves as the hardware carrier of the "error feedback" in NLMS. Since this formula is roughly similar to equation (2), no further elaboration will be provided [5,7].

The NLMS coefficient update module serves as the linchpin for the “adaptive” characteristic. In the context of academic research, the hardware design must be tailored to align with the coefficient update formula [7]:

$$w\left(n+1\right)=w\left(n\right)+\mu\ \frac{e\left(n\right)x\left(n\right)}{P\left(n\right)+\delta} \tag{6}$$

The only difference from the LMS module is the dynamically modulated step-size parameter μ and real-time input signal power calculation and update P(n). To prevent division by zero, we apply a regularization parameter δ=10\^ -6. This methodology prevents the appearance of large fluctuation distortion typical of the IIR method, caused by a constant step size μ and a periodic update of P(n).From equation (6), it may be concluded that hardware implementation of NLMS module consists of three basic components: power estimation unit, step-size adaptation unit and coefficient update unit. The expression for the power estimation unit is [7]:

$$P\left(n\right)=\sum_{k=0}^{N-1}x^2\left(n-k\right)+\delta \tag{7}$$

In the above, x(n-k) is the delayed input signal stored in the feedforward delay chain, where the signal and also the delay signal that is used for FIR filtering is stored to avoid unnecessary redundancy. The small positive constant δ is used to prevent division overflow when the denominator P(n) is nearly equal to 0.It is a multiplier and an accumulator which performs multiplication of the squared magnitude of x(n) and accumulates it in 1 msec, corresponding to 48 samples, to calculate P(n). The operation frequency is synchronized with a 48 kHz sampling rate.

The fundamental principle of the step adjustment unit is to divide the fixed reference step size μ_0 by the real-time power P(n), thereby achieving adaptive normalization of the input signal amplitude. The formula is [7]:

$$\mu\left(n\right)=\frac{\mu_0}{P(n)} \tag{8}$$

Here, μ_0 is the preselected value of the reference step size that must be decided beforehand according to the system stability criterium (to ensure the convergence). When, for example, the input signal x(n) amplitude increases (because of a sudden noise rise etc.), the value of P(n) increases, too, thereby forcing μ(n) to automatically decrease. This mechanism prevents from excessive large values of coefficient update, which may cause divergence. Similarly, we perform the macroscopic coefficient update in the other direction to ensure that the coefficient updates are effective [7]. This

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task is implemented by the coefficient update block, which implements equation (6) to perform the macroscopic coefficient update.

These three basic blocks work collaboratively to provide the algorithmic functions of the NLMS coefficient update block. As one limitation of the IIR method, a large amplitude fluctuation of ambient noise leads to audio quality distortions. The NLMS algorithmic process updates the coefficients effectively and reflects complex surroundings; also they work better to accommodate the real-time process constraints and to meet the high accurate requirement for noise suppression applications.

3. Comparison of performance, cost and power consumption of digital circuits

The hardware difference of the two methods is evaluated by a quantitative measurement and comparison of three dimensions, including performance, cost and power consumption, according to measurement results from previous work, as it can serve as a guiding source for choosing proper headphone for different applications. All the results are reported in Table 1 below.

Table 1. A comparison of the core dimensions of the two schemes

Dimension	Metric	FIR + NLMS [16-19]	IIR + LMS [20,21]
Performance	Low-frequency noise reduction amount (200–250 Hz)	41.65 dB @200 Hz; 31.27 dB @250 Hz	Overall improvement of approximately 7 dB
	Mid-frequency noise reduction amount (500 Hz)	10.56 dB	—
	High-frequency noise reduction amount (≥1 kHz)	The active component plays a relatively minor role, mainly depending on passive sound insulation.	The level of active involvement is restricted.
Cost	Chip size	1.62 mm² (including SRAM≈0.75 mm²,0.35μm CMOS)	0.0185 mm² (precise) 0.0076 mm² (approximate) (45nm CMOS)
	Quantity of multipliers	Exhibits a linear increase with the order of the FIR	Each pair of second-order, time-division multiplexing saves numerous multipliers.
Power Consumption	Total power consumption	247.5 μW (Gammatone, 0.35μm, 1.1V, 0.96 MHz) 0.37 mW (IFIR, 65 nm)	526.19 μW (precise) 203.75 μW (approximate)

In terms of performance, it is the clear advantages of FIR+NLMS method in achieving accurate noise reduction and high fidelity, as it achieves 31.27–41.65 dB noise reduction in low frequency of the critical audio signal, much better than 7dB (the performance of IIR method) and also reduce the low frequency disturbances from air conditioner and sub way system [16,19]. At the medium frequency range, it can realize an improvement of 10.56 dB and satisfy the high-end customer's

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demand on noise cancellation and naturalness of the sound [16]. With the same effect at high frequency as FIR, the overall performance of IIR at the entire frequency band is still unsatisfactory and more appropriate for the low-end application of general noise suppression.

In cost term, IIR+LMS, due to its recursion structure and resource reuse, enjoys high economy which also makes it less costly for implementation. It was implemented in CMOS technology with a process size of 40nm. It has a small chip area about 0.0076 mm2 (or say 0.0185 mm2 is the precise footprint) [21]. Moreover, our solution presents great reduction of hardware resources via time-division multiplexing based multiplier reduction techniques and block-reuse-based standard cell register replacement methods for SRAM blocks. For the above reasons, our solution can be deployed on affordable earphones with a price under 300 CNY to gain a competitive price advantage in price-sensitive consumer electronic products [13,15]. In contrast, our FIR+NLMS implementation is in the 0-structure with 16 taps. However, due to the implementation on a 0.35 μm CMOS process, it requires 16×16-bit SRAM and 1.62 mm² chip area. Meanwhile, with filter order increasing, the needed multipliers follow lineally, therefore, brings out higher cost in total. Thus, it is suitable for premium price-headphones sold in more than 1000 CNY.

Power usage and battery life illustrate the clear difference between the two implementations. While leveraging algorithmic optimization (e.g., calculating the overall power once rather than for each sample), clock gating, and multiplier sharing, the overall power consumed by the IIR design ranges from 203.75 μW to 526.19 μW. This is approximately 909 h with 50 mAh battery, which significantly mitigates the issues of battery life for wireless earphones users [18]. On the other hand, though 0.37 mW is also feasible with FIR by adopting IFIR architecture (in 65nm tech.), it can even be minimized to 247.5 μW by using Gammatone structure. However, as this solution uses 35 μm technology, its total energy efficiency is lower than the IIR solution leading to a lower battery life. For this reason the technology is more suited for high end devices where battery size is less a design constraint [21].

4. Conclusion

In this paper, two common types of digital filters widely utilized in headphone NC systems (the FIR combined with NLMS and IIR with simplified LMS algorithm) are studied in terms of how they are implemented on hardware, what performance bottleneck is there, and what the compatible products are for those digital filters. For a better comparison between the two mentioned digital filters, a series of performance evaluation from four views (noise attenuation accuracy, hardware usage, power consumption and application scenarios) has been done. This shows that the FIR-based solution is the ideal choice for premium, high-end devices, and that the IIR-based solution suits cost sensitive entry-level devices more appropriately.

As to future trends, hardware implementation of filtering algorithms evolve into two main directions. One is to enhance adaptability and reconfigurability. Such adaptability consists of varying the filter order and algorithm step size through programming registers on the run so that the same integrated circuit can deal with varying signal conditions, e.g. background-noise to impulse noise. Second, progress is inspired by advanced fabrication process along with novel circuit level tricks like extreme-low voltage computing blocks and dynamic clock gating, that together diminishes power consumption and signal latency while enhancing processing rate. Such complementary improvement enables a desirable compromise between performance and cost and promotes the deployment of adaptive filtering algorithms in more affordable consumer electronic products.

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