Proceedings of CONF-FMCE 2025 Symposium: Semantic Communication for Media Compression and Transmission
DOI: 10.54254/2755-2721/2025.GL28996

The Impact of Power Consumption of Silicon-based Logic Devices on the Performance of Modern Electronic Systems

Luning Ye

School of Electrical Engineering and Artificial Intelligence, Xiamen University of Malaysia, Selongor, Malaysia
EEE2409050@xmu.edu.my

Abstract. Silicon logic devices are the core of modern electronic systems. As electronic system performance, miniaturization, and multi-functionality increase, their integration and operating frequency increase exponentially while power consumption has doubled significantly, limiting device battery life considerably, generating heat that deteriorates performance/reliability, and being a design bottleneck for electronic systems. This paper investigates the impact of power consumption in silicon-based logic devices on the performance of modern electronic systems and clarifies three primary issues: explaining the processes of dynamic, static, and short-circuit power consumption and their correlation with parameters; analyzing the impact of power consumption on system performance indicators and typical situations; and studying power reduction methods from technical (manufacturing process, circuit design, power management) and design (layout optimization, smart power control) perspectives. With case studies, this research finds that dynamic power usage increases with power supply voltage and operating frequency squared, and static power usage is exacerbated by transistor leakage; high power usage reduces computational speed, energy efficiency, stability, and signal precision; and new processes (5 nm GAA), DVFS, and power gating are effective in managing power and performance. The study provides practical recommendations for power reduction solution development, improving battery life in mobile devices, lowering the cost of data centers, improving IoT stability, and enabling the development of AI, IoT, and 5G technology.

Keywords: Silicon-based logic devices, Power consumption, Electronic system performance, Low-power optimization, Application scenarios

1. Introduction

Silicon-based logic devices form the core of modern electronic systems, driving the advancement of electronic technology. As electronic systems pursue higher performance, smaller size, and richer functions, silicon-based logic devices pack in more transistors and run at higher clock speeds—power consumption climbs steeply. This limitation impacts the operational endurance of electronic systems—such as reduced battery life in mobile devices—and generates substantial heat. Inadequate thermal management can degrade device performance and reliability, potentially leading to system failures.

© 2026 The Authors. This is an open access article distributed under the terms of the Creative Commons Attribution License 4.0 (https://creativecommons.org/licenses/by/4.0/).

DOI: 10.54254/2755-2721/2025.GL28996

Investigating the impact of silicon-based logic device power consumption on electronic system performance holds significant importance. Theoretically, refining the theoretical framework for electronic devices provides support for research, development, and design. In practical applications, clarifying the relationship between power consumption and performance enables the identification of methods to reduce power consumption and enhance performance. This extends device runtime, improves user experience, lowers costs, and reduces energy consumption and carbon emissions. Furthermore, reducing power consumption and enhancing performance are critical for advancing emerging technologies like artificial intelligence, the Internet of Things, and 5G communications. This provides essential hardware support, enabling smooth operation of AI devices, stable IoT functionality, and high-speed, reliable 5G transmission.

When investigating the impact of silicon-based logic device power consumption on modern electronic system performance, literature collection and research methodology are paramount, laying the foundation for the study. This paper employs multiple research methodologies, utilizing circuit theory and semiconductor physics to construct theoretical models. It analyzes the principles, parameters, and intrinsic relationships between silicon-based logic device power consumption and system performance. Case studies examine representative systems like smartphones and data centers, dissecting the impact of power consumption on system performance in real-world scenarios to inform strategy development.

2. Theoretical foundations of power consumption in silicon-based logic devices

2.1. Review of research on power generation mechanisms

The power consumption mechanism of silicon-based logic devices is quite complex, fundamentally driven by multiple internal physical effects.

First is dynamic power consumption, which occurs during device state transitions. When switching between logic levels, current flows through transistors to charge and discharge load capacitance. This process consumes energy, generating dynamic power consumption. Its magnitude is proportional to the device switching frequency, load capacitance value, and the square of the supply voltage. Today, as electronic system operating frequencies continue to increase, dynamic power consumption accounts for an increasingly larger proportion of total power consumption.

Second is static power consumption. Even when a device remains in a stable logic state without state transitions, current leakage occurs, generating static power consumption. This is primarily caused by factors such as transistor subthreshold current and gate leakage current. Subthreshold current refers to the minute current present between the source and drain when the transistor is in a weak inversion state. Gate leakage occurs when electrons penetrate the gate oxide layer due to its limited thickness. As device dimensions shrink, these leakage issues become more pronounced—a 0.5-nanometer reduction in oxide thickness increases gate leakage by an order of magnitude [1], making static power a significant consumption source.

Finally, short-circuit power consumption occurs during logic device state transitions. The rising and falling edges of the input signal briefly overlap with the output signal, creating a transient short-circuit path between the power supply and ground. This generates short-circuit current and associated power consumption. Although short-circuit power duration is extremely brief, its cumulative effect in high-frequency, high-speed electronic systems cannot be ignored.

The power consumption mechanisms of silicon-based logic devices encompass dynamic power, static power, and short-circuit power. These power sources interact with each other, collectively determining the overall power consumption level of the device.

DOI: 10.54254/2755-2721/2025.GL28996

2.2. Review of power consumption-related parameters research

Power supply voltage critically influences power consumption, with dynamic power typically proportional to its square. Reducing voltage effectively lowers dynamic power by minimizing charging/discharging energy, yet excessive reduction can compromise operating speed and reliability. Thus, practical design necessitates a balance between power efficiency and performance integrity.

Operating frequency also significantly impacts dynamic power consumption. Higher frequencies increase switching activity and capacitor cycling, raising power demand—particularly in high-speed systems such as modern processors.

Transistor threshold voltage plays an equally essential role. While a lower threshold reduces dynamic power, it exacerbates subthreshold leakage, elevating static consumption. Optimal power management therefore requires precise threshold calibration to balance dynamic and static power components.

Table 1. Parameter adjustment trade-off comparison table

Parameters	Approaches to Reducing Power Consumption	The performance overhead it brings	Applicable Scenarios
Operating Voltage	Decrease (e.g., from 1.8V to 1.2V)	Device switching speed has decreased (approximately 15% to 25%)	Low-load scenarios (e.g., mobile phone standby)
Operating Frequency	Decrease (e.g., from 5GHz to 3GHz)	Data processing throughput has decreased (approximately 40%).	IoT sensors (low real-time requirements)
Threshold Voltage	Increase (e.g., from 0.3V to 0.5V)	The conduction current decreases, and the drive capability declines.	Scenarios with high static power consumption (e.g., idle servers)

In electronic system design, these power-related parameters of silicon-based logic devices are interrelated and interact with one another. As shown in Table 1, achieving the goals of reducing power consumption and enhancing system performance requires simultaneous consideration of parameters such as supply voltage, operating frequency, threshold voltage, and capacitance values. This can be accomplished through rational design and optimization strategies.

3. The impact of silicon-based logic device power consumption on modern electronic system performance

3.1. Research on system performance metrics

The power consumption of silicon-based logic devices significantly impacts multiple performance metrics of modern electronic systems. A thorough analysis of this impact holds substantial practical value for optimizing electronic system performance and advancing electronic technology.

Regarding computational speed, increased power consumption in silicon-based logic devices exacerbates device heating. Excessive temperatures reduce electron mobility, prolonging logic gate switching times and ultimately slowing overall system processing speed. Taking high-performance computing chips as an example, as logic device power consumption rises, the chip's clock frequency must be reduced to ensure stable operation. This directly impacts data processing speed and efficiency. Conversely, effectively lowering power consumption accelerates logic gate switching speeds, enabling systems to complete complex computational tasks in shorter timeframes and significantly boosting overall processing speed.

DOI: 10.54254/2755-2721/2025.GL28996

Energy efficiency represents a critical performance metric directly shaped by the power consumption of silicon-based logic devices. High power consumption forces systems to expend extra energy, increasing operational costs and limiting deployment in power-constrained applications such as portable electronics and IoT nodes. It also significantly shortens battery life, impairing practical usability. Conversely, reducing power consumption enhances overall energy efficiency, extends operational duration, and enables more sustainable energy use in electronic systems.

Furthermore, system stability is closely linked to power dissipation. When the heat generated by power consumption is not effectively removed through cooling mechanisms, it accumulates, leading to elevated operating temperatures. This overheating can result in performance degradation or permanent hardware damage, thereby jeopardizing the reliability and stability of the entire system.

3.2. Impact analysis of system application scenarios

The power consumption of silicon-based logic devices plays a complex and critical role in the performance of modern electronic systems across various usage scenarios. Below is an in-depth analysis based on several typical scenarios.

In the mobile electronics sector, the rapid advancement of mobile internet has made smartphones, tablets, and other mobile devices indispensable tools in daily life. These devices demand exceptional battery endurance, and as core components, the power consumption of silicon-based logic devices directly impacts battery life. High power consumption means faster battery depletion, which not only shortens user operating time but may also compromise overall device stability. The dynamic power consumption of smartphone chips is directly correlated with data processing intensity. In CMOS circuits, a 50% increase in signal change rate leads to a 30% rise in dynamic power consumption. Furthermore, inrush current and short-circuit current can leak data information. Addressing this requires N-type dynamic circuit design to reduce power consumption while ensuring security and extending battery life [2].

In data center scenarios, the power consumption of silicon-based logic devices is also a significant issue. Data centers handle massive amounts of data storage, processing, and transmission, requiring continuous operation of numerous servers. Silicon-based logic devices account for a substantial portion of total data center energy consumption. High power consumption not only increases operational costs but also poses significant challenges to data center cooling systems. Ensuring equipment functionality requires substantial resources for thermal management, further amplifying energy usage. Moreover, excessive power consumption may accelerate equipment aging, heightening hardware failure risks and compromising data security and reliability —ultimately undermining data center stability and service quality. Silicon-based logic devices account for 60%-70% of total data center energy consumption. For every additional 1kW of device power consumption, an extra 0.3-0.5kW of cooling energy (e.g., air conditioning, liquid cooling systems) is required, increasing annual operating costs by approximately 12,000-18,000 yuan [3].

In IoT applications, numerous sensor nodes and smart devices require long-term stable operation. The low-power characteristics of silicon-based logic devices are critical for the endurance and reliability of these devices. Excessive power consumption may necessitate frequent battery replacements or charging for IoT devices. Furthermore, high power consumption can cause communication delays or errors between devices, impairing the data transmission and processing efficiency of the entire IoT system and hindering the widespread adoption of IoT applications. The endurance bottleneck for IoT sensor nodes centers on energy consumption during the access process and idle listening losses. In traditional 6TiSCH industrial wireless sensor networks, channel scanning and broadcast interactions during node joining consume substantial energy, while the

DOI: 10.54254/2755-2721/2025.GL28996

continuous downlink signal monitoring during idle periods leads to inefficient power expenditure. Kim et al.'s ultra-low-power 6LPN (6TiSCH Low-Power Node) solution reduces node join-phase energy consumption by 90% through: - Reducing advertised channel count (from 8 to 2) - Optimizing scan duration (from 500ms to 80ms) - Implementing delayed join mechanisms simultaneously, by caching downlink data via 6FN (6TiSCH Friend Node), idle listening is entirely eliminated, reducing operational phase power consumption by 87%-94% while maintaining an average data latency of just 7.62 seconds. This perfectly aligns with the low-maintenance requirements of remote sensors in industrial IoT applications (e.g., agricultural monitoring, equipment maintenance nodes) [4].

The power consumption of silicon-based logic devices impacts system performance in multiple ways across different application scenarios. Gaining a deep understanding of these impacts is crucial for optimizing system design, enhancing system performance, and advancing related fields. In diverse scenarios such as mobile electronics, data centers, and IoT, the power consumption of silicon-based logic devices must be prioritized, with effective measures implemented to reduce power consumption, ensuring stable system operation and robust performance.

4. Review of strategies for reducing power consumption in silicon-based logic devices to enhance system performance

4.1. Technical strategy research

Reducing power consumption in silicon-based logic devices is pivotal for advancing electronic systems. Key technical strategies at the device level include employing advanced nanoscale processes to minimize capacitive losses and leveraging novel high-mobility semiconductor materials to enhance electron transport efficiency. Further optimization of material lattice structures and doping profiles can also significantly improve electrical performance and lower power consumption. In advanced processes, self-aligned vertical nanoring gate structures achieve dynamic threshold voltage adjustment through the backside effect. This reduces leakage current while increasing on-state current (FD-SOI-HC VNWFET on-state current increased by 22%), providing a new pathway for low-power manufacturing of nanoscale silicon-based devices [5].

Innovations in circuit design technology are equally crucial for reducing power consumption. Dynamic Voltage and Frequency Scaling (DVFS) technology dynamically adjusts supply voltage and operating frequency in real-time based on system workload. During light-load conditions, voltage and frequency are lowered to minimize power consumption; under high-demand scenarios, they are restored to higher levels to ensure performance. This adaptive approach effectively balances performance and power consumption. Beyond this, low-power logic gate design has garnered significant attention. Developing novel logic gate circuit structures and adopting more efficient logic operation methods reduce unnecessary signal flips, thereby achieving power savings.

A comprehensive methodology addressing device manufacturing, circuit architecture, power management, and thermal control enables substantial power reduction in silicon-based logic devices, creating pathways toward next-generation high-performance, low-power electronic systems.

4.2. Design-level strategy research

In research aimed at enhancing the performance of modern electronic systems, reducing the power consumption of silicon-based logic devices is a key direction, and design-level strategy research is

DOI: 10.54254/2755-2721/2025.GL28996

particularly crucial. Approaching the issue from a design perspective allows for fundamental control over power consumption, thereby improving overall system performance.

Optimizing circuit layout design is a vital means of reducing power consumption. A well-planned layout minimizes signal transmission distances and interference, thereby reducing energy consumption. During design, modules should be scientifically arranged based on the functionality and signal flow of silicon-based logic devices. For instance, frequently interacting modules should be placed close together to shorten signal paths, reducing transmission delays and power consumption. Employing a hierarchical layout—separating circuits with different functional levels—not only improves circuit stability and maintainability but also contributes to power reduction.

Power management design is equally critical at the design level. Intelligent power management strategies dynamically adjust power supply based on system operating conditions. For instance, during low-load operation, reducing the supply voltage to silicon-based logic devices lowers power consumption. When high computational performance is required, the supply voltage can be restored to normal levels. Additionally, implementing power gating technology cuts power supply to logic devices when they are temporarily inactive, preventing static power consumption. Power optimization for silicon-based components in data centers requires integration with intelligent scheduling. Pre-cooling strategies utilize redundant renewable energy to eliminate “hotspots,” preventing performance throttling caused by localized overheating while reducing compensatory power consumption [6].

5. Conclusion

Extensive research has meticulously mapped the landscape of power dissipation in silicon-based logic devices, spanning from transistor switching dynamics to circuit leakage currents. These studies have successfully delineated the respective contributions of dynamic and static power across operating modes, establishing a fundamental framework that informs and enables targeted strategies for power reduction.

Research on parameters related to power consumption has also made significant progress. The relationship between many parameters—such as voltage, frequency, and transistor size—and power consumption has been carefully studied. Research indicates that appropriately adjusting these parameters can reasonably optimize the power consumption of silicon-based logic devices. Existing advanced process studies have confirmed the correlation between “size reduction and power reduction.” TSMC's 5nm process further optimizes the power-performance ratio through structural upgrades from FinFET to GAA. However, the increased manufacturing costs and thermal challenges brought by process upgrades remain issues that future research must address [7].

Future research directions are extensive. It is essential to delve deeper into the intrinsic relationship between power consumption and system performance, establishing more comprehensive and precise multidimensional performance evaluation models. Further investigation is needed into the power stability of such devices in complex electromagnetic environments to adapt them to high-frequency scenarios like 5G communications [8].

References

[1] Min Shi, Guojue Wu. (2008) Semiconductor Device Physics [M]. Xi’an: Xi’an Jiaotong University Press, pp. 215-230.

[2] China Science and Technology Paper Online. Integrated circuit chip instantaneous power measurement - acquisition - analysis system [EB/OL]. http: //www.paper.edu.cn/scholar/shpaper/MUz2YNxINTj0gx1h, 2025.

DOI: 10.54254/2755-2721/2025.GL28996

[3] Future Think Tank. (2024) 2024 Special Report on Liquid Cooling Industry in Data Centers [R]. Beijing: Future Think Tank.
[4] Kim J., Lee S., Park H. (2024) Supporting Ultralow-Power Nodes in 6TiSCH Industrial Wireless Sensor Networks [J]. IEEE Internet of Things Journal, 11(23): 38337-38347.
[5] Huilong Zhu, et al. (2022) Self-aligning gate vertical nanocyclic gate transistor with dynamically adjustable threshold voltage [J]. J. Semicond., 43 (1): 014101.
[6] Jiantao Zhou, et al. (2025) A Reinforcement Learning Based Framework for Holistic Energy Optimization of Sustainable Cloud Data Centers [J]. IEEE Transactions on Services Computing (TSC).
[7] TSMC. (2023) White Paper on Power Consumption of 7nm vs 5nm Advanced Processes [R] Taiwan, China: TSMC Corporation.
[8] Convertino C., et al. (2021) A hybrid III–V tunnel FET and MOSFET technology platform integrated on silicon [J]. Nature Electronics.