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The Progress, Application and Challenges of Carbon Nanotube Transistor Technology

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Abstract. Transistors are at the core of electronic technology, but traditional silicon-based transistors are facing performance bottlenecks. Carbon nanotubes (CNTs), with their excellent electrical properties and nanoscale dimensions, have become the ideal material for the next generation of transistors. This article reviews the fundamental characteristics of carbon nanotube semiconductor materials, their significant advantages over traditional silicon-based materials, the progress in transistor research and their application fields, as well as the existing challenges and problems faced by carbon nanotube transistors. The paper mainly introduces the preparation process of carbon nanotubes, the innovation of device structure, and the optimization strategies for electrical properties. In addition, the article also explores the application potential of carbon nanotube transistors in fields such as integrated circuits, radio frequency electronics, display technology, high-performance computing, and sensors. Finally, this paper points out that the issues of purity control, high-frequency performance bottleneck, and integration uniformity still need to be further addressed. It also looks forward to the improvement methods and future development directions for the difficulties it faces, providing a reference for the practical application of carbon nanotube transistors.

Keywords: Carbon nanotube semiconductor materials, transistors, integrated circuits, sensors

1. Introduction

Transistors are the foundation of modern electronic technology. However, traditional silicon-based transistors are facing physical limitations and power increase issues when it comes to size reduction, which has made them unable to meet the current demands for high performance, miniaturization, and low power consumption. Carbon nanotubes, due to their excellent electrical properties, nanoscale size, and low power consumption characteristics, have become an ideal choice for the next generation of transistor materials.

In recent years, global researchers have made significant progress in the preparation of carbon nanotubes, the optimization of devices, and the integration of circuits. For instance, the research team from Peking University successfully prepared an ultra-high purity carbon tube solution through multiple polymer dispersion and purification techniques. By combining the dimensionally constrained self-arrangement method, they fabricated a high-density, high semiconductor purity

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carbon tube array on a 4-inch substrate. They also batch-produced field-effect transistors and ring oscillator circuits, demonstrating excellent performance. Compared with silicon-based CMOS devices and circuits of similar size, the static power consumption was reduced by 80.18%, and the dynamic power consumption was reduced by 21.80% [1]. Furthermore, significant breakthroughs have been achieved in the research on interface states of carbon nanotube transistors, chirality control, and their applications in analog circuits and digital circuits [2-4]. However, there are still many challenges for carbon nanotube transistors to move from laboratory research to practical applications, such as the large-scale preparation technology of carbon nanotubes, the stability and reliability of the devices, etc., which remain to be solved.

This article will conduct a comprehensive review of the research progress of carbon nanotube materials in the field of transistors from several aspects: the material basis of carbon nanotubes, the research progress of carbon nanotube transistors, the application fields of carbon nanotube transistors, as well as the current problems and challenges. The aim is to summarize the current research status, analyze the challenges faced, and look forward to the future development trends.

2. Basics of carbon nanotube semiconductor materials

2.1. Basic structure and characteristics

Carbon nanotubes (CNTs) are one-dimensional quantum materials composed of hexagonal carbon atoms. Their diameters are typically between 2 and 20 nm. Single-walled carbon nanotubes can be formed by rolling up a single graphene sheet. They can be classified by the number of layers as single-walled carbon nanotubes (SWCNT) and multi-walled carbon nanotubes (MWCNT), and by structural characteristics as chair-like (n = m), zigzag-like (n > m = 0), and chiral (n > m ≠ 0) [5]. Figure 1 is a schematic diagram of single-walled carbon nanotubes (SWCNTs). The electrical properties of single-walled carbon nanotubes (SWCNTs) depend on the chirality index (*n, m*). When n=m or n-m=3i (*i* is an integer), they exhibit metallic properties; otherwise, they are semiconductor-like. Their diameters can be calculated using the following formula [5]. $DCNT = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2+m^2+nm}$, here, a_0 = 0.142 nm, and *n, m* are chirality indices.

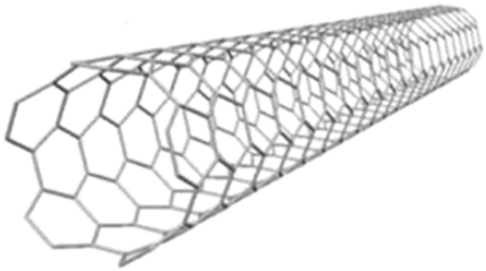


Figure 1. Single-walled carbon nanotube [6]

Figure 2 is a schematic diagram of a carbon nanotube transistor. In the carbon nanotube field-effect transistor (CNTFET), the semiconductive single-walled carbon nanotubes serve as the conductive channel and are compatible with the MOSFET structure, enabling integration into CMOS designs [6]. CNTFET exhibits high electron mobility, customizable threshold voltage, and excellent thermal conductivity, which can significantly enhance device performance and reliability [6].

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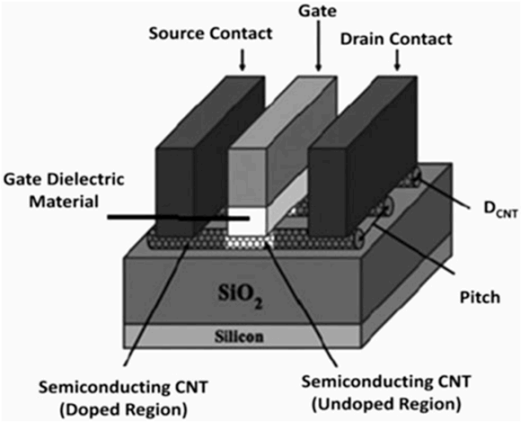


Figure 2. Schematic diagram of CNTFET using multiple carbon-type nanotubes in the channel [5]

2.2. Compared with traditional silicon-based materials

With the continuous miniaturization of semiconductor process dimensions, traditional silicon-based technologies are facing severe challenges such as scalability, leakage current, short-channel effect, and reliability. Especially at technology nodes below 32nm, CMOS transistors are constrained by multiple factors, including short-channel effect, high leakage power, and process variability sensitivity. In contrast, carbon nanotube technology demonstrates significant advantages. The adder based on CNTFET outperforms the CMOS adder in key indicators such as power consumption, delay, and power-delay product (PDP). The experimental data show that within the operating voltage range of 0.8V to 1.2V, the power consumption of the CNTFET adder is reduced by over 73%, the delay is decreased by over 29%, and the power-delay product (PDP) is optimized by over 81%. Within the temperature range of -25°C to 75°C, the power consumption is reduced by over 64%, the latency is decreased by more than 19%, and the power-delay product (PDP) is improved by over 71% [6]. In conclusion, carbon nanotube technology demonstrates great potential for development and is expected to become an important path for maintaining the performance improvement of integrated circuits in the post-Moore era.

3. Research progress of carbon nanotube transistors

3.1. Preparation process of carbon nanotubes

The common methods for preparing carbon nanotubes include chemical vapor deposition (CVD) and solution dispersion and purification.

Two-dimensional single-walled carbon nanotube (SWNT) arrays can be directly grown on hexagonal boron nitride (hBN) substrates through catalytic chemical vapor deposition. The specific process is as follows: first, catalytic iron nanoparticles are deposited on the hBN/SiO_2/Si substrate; then, the substrate is heated to 850°C in an argon/hydrogen mixed atmosphere, and methane is introduced as the carbon source to grow for 60 minutes; finally, it is cooled to room temperature under a protective atmosphere [3]. The chemical vapor deposition method is more suitable for the fabrication of high-performance and high-integration CNT electronic devices, especially in scenarios that require high orientation, high density, and uniform chirality.

High-purity semiconductor carbon nanotubes can be prepared through multiple steps of centrifugation and solvent treatment. For instance, the raw carbon nanotubes obtained by the arc

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discharge method are mixed with conjugated polymer PCz in toluene. After ultrasonic dispersion, gradient centrifugation (20,000 - 50,000 g) and vacuum filtration, a carbon nanotube solution with semiconductor purity > 99.999% is obtained. Further, through dynamic liquid phase filtration and dip-coating processes, a uniform array of carbon nanotubes can be formed on a 4-inch wafer [1]. The solution dispersion and purification method is more applicable to large-scale, low-cost, and flexible electronic applications, especially in cases where high-purity semiconductor CNTs are required. The two methods can be used complementarily. The solution dispersion and purification method provides high-purity CNT raw materials, while the chemical vapor deposition method is used to directly grow high-quality arrays on specific substrates, jointly promoting the development of carbon nanotube electronic technology.

3.2. Innovative device structure

3.2.1. Foundation structure design

The basic structural designs of carbon nanotube crystals include back-gate structure, top-gate structure, and surrounding-gate structure. The back-gate structure achieves high switching ratio performance by optimizing the channel and dielectric layer. In the research by Khan et al. on the back-gate SWCNT FET, a silicon substrate was used in combination with a SiO_2 dielectric layer (100 nm), along with Ti/Pd (5 nm/25 nm) source and drain electrodes. The channel length was optimized to 2 μm [7]. This design regulates carrier transport through the back-gate voltage, significantly enhancing the device's switching ratio (up to 10^8), and is suitable for high-performance field-effect transistor applications [7].

The top-gate and surround-gate structures significantly enhance the gate control capability through the use of high-k dielectrics and three-dimensional gate designs. Liu et al. proposed a top-gate structure that uses atomic layer deposition (ALD) to fabricate a HfO_2 high-k dielectric layer (15 nm), resulting in an approximately 40% increase in gate control efficiency and effectively reducing the sub-threshold swing to 215 mV/dec [8]. The surround-gate structure, by enclosing the channel with a three-dimensional gate, suppresses the leakage current to below 10 nA/μm, significantly alleviating the short-channel effect [8].

3.2.2. Development of new structures

The development of new structures includes suspended pre-stressed structures, fully-contact structures, and asymmetric gate structures. The performance of carbon nanotube sensors is significantly improved through the use of the suspended pre-stressed structure. Bottger et al. achieved controllable pre-stretching (0.42% - 0.95%) of carbon nanotubes by designing the residual stress of Si_3N_4/SiO_2 films, significantly enhancing the sensitivity (gauge factor reaching 644 ± 250) of the strain sensor, providing a new solution for miniaturized high-sensitivity strain detection [9].

The use of a fully contact structure significantly reduces the contact resistance of carbon nanotube transistors. Lin et al. proposed that this structure achieves this by simultaneously forming side and end contacts between the metal and the carbon nanotubes, reducing the contact resistance to 90 Ω·μm and significantly reducing the dependence on the contact length [1]. Even when the contact length is reduced to 30 nm, it still maintains low resistance characteristics, laying the foundation for the development of devices with a 55 nm contact gate spacing (corresponding to a 10 nm technology node) [1].

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The RF performance is optimized through the synergy of asymmetric gate structure and selective doping. Ren et al. proposed to optimize the spacing ratio of the gate-source (S-spacer) and gate-drain (D-spacer) (such as 1:1, 1:3, 1:5), and combine the selective doping of palladium (Pd) particles in the drain region, effectively reducing the access resistance, and increasing the cut-off frequency (f_t) and the maximum oscillation frequency (f_{max}) of the device by 1.3 times [10].

3.3. Electrical performance optimization strategy

There are three strategies for optimizing electrical performance: interface state regulation, doping and passivation, and process optimization.

By optimizing the gate dielectric process, the performance of the device can be significantly improved. For instance, Si et al. proposed using oxygen-enhanced atomic layer deposition (ALD) technology to grow HfO_2 gate dielectric, and combined with H_2O pre-treatment to increase the nucleation sites, which can effectively reduce oxygen vacancies and reduce the interface state density (D_{it}) to 6.1×10^{11} $cm^{-2}eV^{-1}$. At the same time, it achieves excellent performance, such as a transconductance (g_m) of 2.42 mS/μm and a switch ratio of 10^5 [4].

Selective doping is an effective method for improving contact characteristics. Ren et al. proposed introducing 0.3-0.5 nm Pd particles into the drain region and combining it with an asymmetric gate structure design, which could increase the current density by 2-3 times. This strategy achieved a cutoff frequency (f_t) of 52 GHz and a maximum oscillation frequency (f_{max}) of 63 GHz at a 400 nm channel length [10].

The surface treatment process has a crucial impact on the performance of the devices. Zhang et al. proposed that by performing vacuum annealing (at 400°C) and oxygen plasma etching to remove the residual polymers on the surface of carbon nanotubes, the interface scattering could be reduced, enabling the carrier mobility of 30 nm gate-length devices to remain at 500 $cm^2V^{-1}s^{-1}$, which is superior to that of silicon-based devices at the same technology node [3].

4. Application fields of carbon nanotube transistors

4.1. Integrated circuits and digital circuits

Integrated circuits based on carbon nanotube field-effect transistors (CNTFETs) have demonstrated significant advantages in the field of digital circuits. In the aspect of logic circuits, Anjaneyulu et al. proposed the implementation of an 11T full swing structure CNTFET adder as shown in Figure 3. At the 32 nm technology node, compared with the CMOS implementation, its power consumption is reduced by 73%, the delay is decreased by 29%, and the power-delay product (PDP) is reduced by 81%, which is particularly suitable for low-power, high-speed arithmetic operation scenarios [6].

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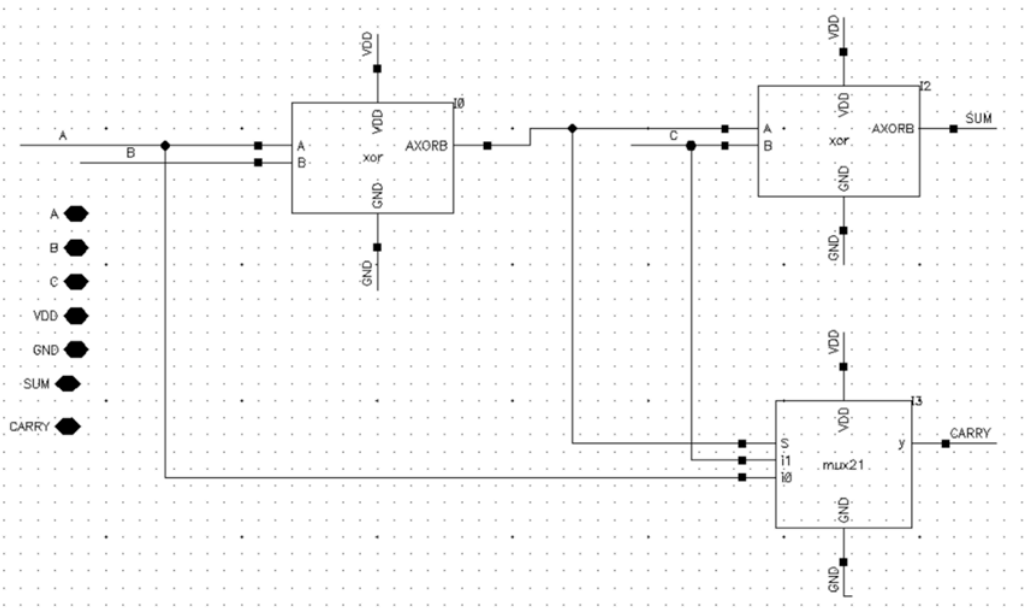


Figure 3. CNTFET implementation of the full swing 11T adder [6]

In the design of storage units, Lin et al. proposed a static random access memory (SRAM) unit based on CNTFET, with the area reduced to 0.976 μm², which is comparable to the 90 nm silicon-based technology node. At the same time, the static and dynamic power consumption were reduced by 80.18% and 21.80% respectively, providing a new solution for high-density integration [1].

Furthermore, carbon nanotube technology has also been applied in the field of high-performance computing. For instance, Si et al. proposed a tensor processor (TPU) containing 3,000 transistors, which achieves 2-bit integer multiplication and accumulation operations through a pulsating array architecture. It achieved an accuracy rate of 88% in the handwritten digit recognition (MNIST dataset) task, with a power consumption of only 295 μW, demonstrating its great potential in accelerating computing for artificial intelligence [4].

4.2. Radio frequency electronics and communications

4.2.1. High-frequency transistors and amplifiers

Carbon nanotube RF transistors significantly enhance their high-frequency performance by optimizing the device structure (such as the asymmetric gate spacing) and the doping process. For instance, Ren et al. proposed a device with an asymmetric gate structure, which achieved a cutoff frequency (f_T) of 52 GHz and a maximum oscillation frequency (f_{max}) of 63 GHz. The RF amplifier based on such a device increased the conversion gain by 10 dB at 8 GHz (X-band), demonstrating its potential in high-speed wireless communication [10].

Lin et al. proposed that by reducing the contact gate distance to 55 nm, they achieved a carrier injection speed of 1.1×10^7 cm/s at a 30 nm gate length. The performance was superior to that of silicon-based PMOS devices at the 10 nm node, providing new possibilities for terahertz band communication [1].

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4.2.2. Internet of things and sensor interface

The ultra-wideband transmitter based on CNTFET is suitable for wireless communication in the Internet of Things due to its low power consumption and high output power characteristics. Kumar et al. proposed an ultra-wideband (UWB) transmitter based on a carbon nanotube field-effect transistor (CNTFET), which has a power consumption of only 1.069 mW at a data rate of 10 GHz and an output power of 32.27 dB. Its low power consumption and high efficiency make it an ideal choice for inter-chip wireless communication and IoT devices [11].

4.3. Display technology

By optimizing the multilayer gate dielectric and passivation layer, carbon nanotube thin-film transistors significantly enhance the driving performance of Micro-LED displays. In the field of micro-LED display driving, Liu et al. proposed carbon nanotube thin-film transistors (CNT TFT) by adopting an optimized gate dielectric (HfO_2/SiO_2 multilayer) and passivation layer (SiO_2/Y_2O_3 multilayer), which significantly improved the device performance. This design achieved a high switching ratio and low hysteresis voltage, making it an ideal choice for high-resolution display applications [2].

4.4. High-performance computing and 3D integration

The low-temperature processing technology of carbon nanotubes and the three-dimensional integration technology significantly enhance the system energy efficiency and computing performance. Zhang et al. proposed a low-temperature fabrication process for carbon nanotube transistors (<400 ℃) that enables compatibility with silicon-based circuits and realizes three-dimensional heterogeneous integration. This integration method effectively reduces interconnection delay, thereby improving the overall system energy efficiency [3]. Additionally, Si et al. proposed a system-level simulation indicating that an 8-bit carbon nanotube tensor processing unit (TPU) based on a 180nm technology node can achieve a main frequency of up to 850MHz, with an energy efficiency of 1TOPS/W, demonstrating its great potential in high-performance computing scenarios [4].

4.5. Sensor

4.5.1. Biological molecule detection

Carbon nanotube field-effect transistors (CNTFETs) modified by surface functionalization (such as PBASE) can achieve highly sensitive detection of biomolecules. For instance, Zamzami et al. successfully detected the surface spike protein (S1) of SARS-CoV-2 using CNTFETs. The schematic diagram and circuit diagram of the structural components of the CNTFET sensor are shown in Figure 4. The principle is to achieve rapid response through the current change caused by the antibody-antigen binding [12].

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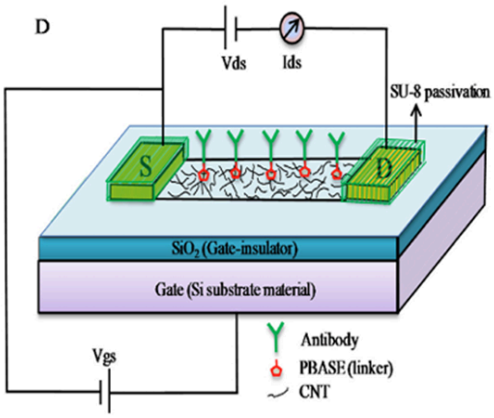


Figure 4. Schematic diagram and circuit diagram of the structural components of the CNT-FET sensor [12]

Furthermore, the research conducted by Villamizar et al. indicates that CNTFET can also be utilized for the detection of molds in food (such as Aspergillus flavus). Even at low concentrations, it demonstrates excellent recognition capabilities, providing a new method for food safety and environmental monitoring [11].

4.5.2. Adaptation and physical sensing

The NEMS sensor based on pre-strained suspended carbon nanotubes achieves high-sensitivity mechanical strain detection and chip-level integration. Bottger et al. developed a NEMS sensor based on pre-strained suspended carbon nanotubes, with a strain coefficient (gauge factor) of up to 644 ± 250, capable of detecting as small as 0.017% of the micro mechanical strain [9]. This sensor is compatible with surface micromachining technology and CMOS process, and can be integrated onto the chip to achieve real-time health monitoring of electronic systems (PHM), especially suitable for fields with strict reliability requirements such as autonomous driving [9].

5. Current issues and challenges

5.1. Purity control

The main difficulty in achieving purity control lies in the interference from semiconductor purity and metallic impurities. Although semiconductor materials have reached a high purity of 99.9999%, the remaining metallic carbon nanotubes can still cause leakage problems in the devices, resulting in a decrease in the switch ratio (I_{on}/I_{off}). This phenomenon is particularly prominent in high-density arrays and requires further reduction of the metal tube content to suppress current crosstalk [3].

Furthermore, during the dispersion and sorting process of carbon nanotube films, polymer residues (such as PCz) can form interface defects. Therefore, high-temperature annealing and wet cleaning processes need to be introduced to eliminate the residues, which, to some extent, increases the complexity of the process.

In the future, the preparation process needs to be optimized to achieve uniform distribution of chiral structures at the wafer scale and high consistency of device performance. At the same time, low-temperature purification technology should be developed to ensure good compatibility with the silicon-based CMOS back-end integration process [4].

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5.2. High-frequency performance bottleneck

The main bottleneck of high-frequency performance lies in the limitations of random orientation carbon nanotube films. Ren et al. pointed out that due to the large parasitic capacitance and resistance of random orientation carbon nanotube films, the cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) of their RF transistors are usually difficult to exceed 100 GHz. In contrast, aligned arrays of carbon nanotubes, although having higher theoretical performance, are still limited in practical applications due to the inter-tube coupling effect and interface scattering problems [10].

In the future, it is necessary to systematically optimize the device structure and doping process, reduce parasitic parameters, and develop more effective interface control and low-damage integration methods to jointly enhance the frequency characteristics and energy efficiency of carbon nanotube RF devices.

5.3. Integration challenge

The integration challenge mainly lies in the issue of uniformity in large-scale integration. Si et al. pointed out that in integrated systems containing more than 3000 transistors (such as carbon nanotube tensor processing units), the fluctuation of threshold voltage (V_{th}) can reach 0.2 V, which significantly increases the risk of circuit functional failure [4]. Therefore, improving the uniformity of materials and processes has become the key to achieving reliable integration.

In the future, the materials and processes need to be further optimized to suppress the Vth fluctuations, improve the wafer-level uniformity, and develop more precise doping and interface control technologies, so as to ensure the reliability and yield of ultra-large-scale carbon nanotube integrated circuits.

6. Conclusion

Research on carbon nanotube transistors has made significant progress in material foundation, device design, and application exploration, demonstrating the potential to surpass traditional silicon-based technologies. By optimizing the fabrication process and device structure, researchers have achieved high-performance and low-power carbon nanotube transistors and have demonstrated their practical application value in digital circuits, radio frequency communication, and sensor fields.

However, there are still numerous challenges for carbon nanotube transistors to move from the laboratory to industrialization, including the leakage of devices and the decline in switching ratio caused by metallic impurities, which require further improvement in purity; in high-frequency applications, parasitic parameters limit their performance and make it difficult to exceed 100 GHz; and during large-scale integration, the threshold voltage fluctuation significantly increases the risk of circuit failure. In the future, these problems need to be solved through collaborative innovation in multiple aspects, such as material preparation, device structure, and process integration. Through interdisciplinary collaboration and technological innovation, carbon nanotube transistors are expected to become the core material of the next-generation electronic devices, injecting new vitality into the continuous development of electronic technology.

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