Proceedings of CONF-FMCE 2025 Symposium: Semantic Communication for Media Compression and Transmission
DOI: 10.54254/2755-2721/2025.GL28000

Research on Short-Circuit Mechanism and Protection Methods of the SiC MOSFETs

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Abstract. Silicon carbide (SiC) MOSFETs are fundamental to the advance of high-efficiency, high-power-density electronic systems, owing to their superior material properties compared to conventional silicon (Si) devices. However, their widespread adoption is hindered by their relatively weak short-circuit withstand capability, which stems from smaller chip sizes and higher current densities. This paper provides a comprehensive review and analysis of the failure modes, underlying physical mechanisms, and protection strategies pertinent to SiC MOSFETs under short-circuit conditions. The second section of the main body in this paper reveals two primary failure modes: gate interlayer dielectric breakdown (Mode I) and thermal runaway (Mode II), which are driven by thermomechanical stresses and parasitic BJT activation, respectively. Furthermore, threshold voltage instability, caused by oxide trap charging and activation, is identified as a significant factor degrading long-term reliability. In the third section, a critical evaluation of short-circuit protection (SCP) methods is presented, categorizing them based on the monitored parameters (VDS, IDS, or gate characteristics). The analysis reveals that while traditional desaturation detection is common, it is often too slow for SiC devices. Advanced methods using Rogowski coils or two-dimensional monitoring offer the requisite ultra-fast detection times (<100 ns) but increase complexity. The necessity of implementing Soft Turn-Off (STO) strategies to safely mitigate destructive voltage overshoots post-detection is also established. This paper synthesizes these findings to offer a holistic understanding of SiC MOSFET short-circuit reliability and provides a crucial guide for designing robust and effective protection systems.

Keywords: SiC MOSFET, short-circuit mechanism, desaturation detection, short-circuit protection

1. Introduction

In comparison to silicon (Si), silicon carbide (SiC) exhibits a wider bandgap, enhanced electron mobility, and superior thermal conductivity. Therefore, it is perceived as a pivotal material for next-generation power electronic devices. SiC MOSFETs demonstrate lower on-state resistance, higher breakdown voltage than Si IGBTs, and elevated junction temperature capabilities. Moreover, the absence of tail current during turn-off in SiC MOSFETs significantly reduces switching losses, thereby enabling higher switching frequencies and improved operational efficiency. SiC-based

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DOI: 10.54254/2755-2721/2025.GL28000

components have gained extensive adoption in applications such as renewable energy systems, motor drive circuits, and high-efficiency, high-power-density switching power supplies [1].

Due to their smaller chip area and higher current density, SiC MOSFETs exhibit weaker short-circuit withstand capability. This captures massive attention and prompts various tests and studies. Research in [2] reveals that short-circuit withstand times vary across manufacturers, with 1.2 kV/300 A (CREE) SiC MOSFETs enduring 1.9μs and 1.2 kV/180 A (ROHM) lasting 7.2μs at 800 V bus voltage. Reference [3] suggests that SiC MOSFET short-circuit protection should activate within 3μs, while [4] demonstrates that higher temperatures or voltages reduce withstand time. Additionally [5], notes that short-circuit duration impacts device reliability, and studies [2-6] recommend pulse blocking within 2μs. Compared to Si IGBTs, which require 10μs for short-circuit protection, SiC MOSFETs demand faster response times. Protection methods are outlined in former studies, including desaturation detection [7-10], inductance current detection [11,12], additional source detection [13,14], Rogowski coil principle [15,16], and VGS/charge detection [8], each with unique strengths and weaknesses. Desaturation detection is the most common in engineering due to its reliability and applicability, but it faces challenges like delayed detection and false triggers at elevated temperatures when used for SiC MOSFETs. To address these, this paper conducts a comprehensive literature review to analyze and summarize recent advancements, categorizing highly effective SiC short-circuit protection methods and identifying the most efficient and versatile approaches, which will be proposed in subsequent sections.

In general, this paper is organized as follows. The short-circuit failure modes and mechanism of the SiC MOSFETs are described in detail in Section 2. The short-circuit protection methods are categorized and studied in Section 3. Finally in Section 4, the approaches mentioned in the former section are evaluated in a comparative way and the conclusions and discussion are drawn.

2. Short-circuit failure modes and mechanism of the SiC MOSFETs

2.1. SiC MOSFETs' threshold-voltage instability

Threshold-voltage (V_T) instability is a primary reliability concern for SiC MOSFETs. It is primarily caused by active charge traps located in the gate oxide, near the semiconductor interface. The phenomenon is governed by two dominant mechanisms: oxide-trap charging and oxide-trap activation [17].

Oxide-Trap Charging: This reversible process involves the charging and discharging of already-existing oxide traps via a direct tunneling mechanism. (See Fig. 1) When a negative gate bias is applied, electrons tunnel out of the traps near the interface, leaving behind positively-charged traps and causing a negative shift in V_T. Conversely, a positive gate bias causes electrons to tunnel back into these traps, neutralizing them and resulting in a positive V_T shift. This process leads to a characteristic hysteresis in the device's I-V curve that increases linearly with the logarithm of the stress time. The observed V_T shift is highly dependent on measurement speed; slower measurements record smaller shifts because traps very close to the interface can change their charge state back during the measurement sweep itself [17].

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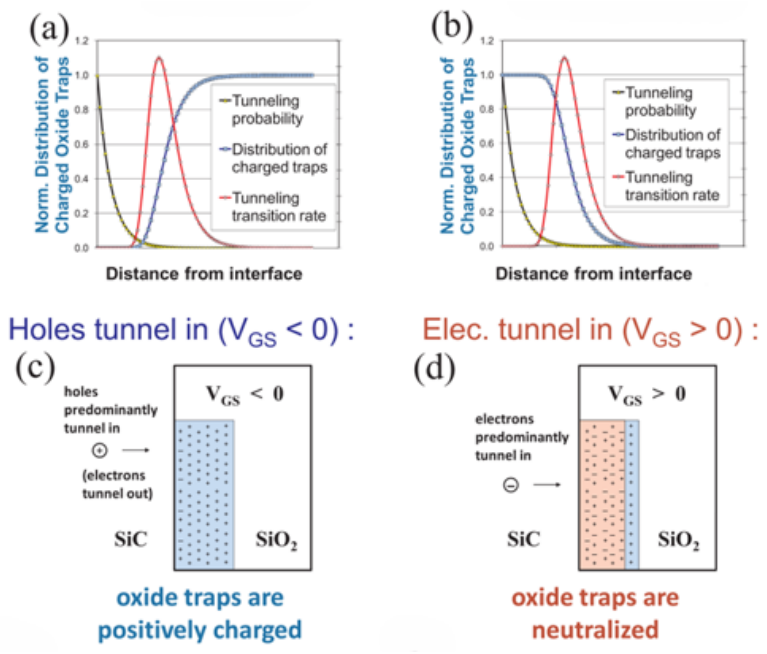

Figure 1. Oxide-Trap Charging mechanism. Schematic illustrating the effect of gate-bias stress on the near-interfacial oxide traps. (c) Under negative gate bias (VGS<0), electrons tunnel out, leaving the traps positively charged. (d) Under positive gate bias (VGS>0), electrons tunnel in, neutralizing the traps. (a) and (b) illustrate the concept of a spatially-peaked tunneling front moving into the oxide from the interface. (Adopted from [17])

Oxide-Trap Activation: This is a degradation mechanism that occurs under prolonged bias-temperature stress (BTS), especially at temperatures above 125°C. An illustration of this is seen in Fig. 2, where the results of a repeating back-and-forth gate-bias stress(1000 s under positive gate bias (+ 15 V), followed by 1000 s under negative gate bias (− 15 V)) at 150 °C are shown for an older-vintage (pre 2014) commercial device. The stress induces the creation of new, active oxide traps that were previously electrically inactive. This effect, which can cause a permanent drift in V_T, has a calculated activation energy of approximately 1.1-1.2 eV. This energy level is consistent with the transformation of neutral Si-dimer states into active E' centers, which are point defects associated with oxygen vacancies in the gate oxide [17]. The instability is ultimately caused by the movement of these interfacial charge traps, which are activated by the high temperatures and high inrush currents present during stress events [18].

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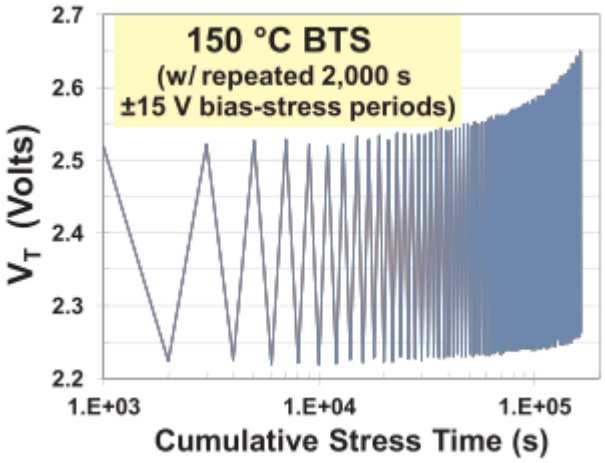

Figure 2. Threshold Voltage Instability under Bias-Temperature Stress (BTS). Experimental results of a repeating back-and-forth bias-temperature stress at 150°C. The expanding envelope of the threshold voltage (VT) over cumulative stress time indicates the activation of new, permanent oxide traps, leading to device degradation. (Adopted from [17])

2.2. Short-circuit failure modes and behavior of the SiC MOSFETs

The behavior of a SiC MOSFET during a short-circuit(SC) event depends on which condition the device is under. Short-circuit events are broadly categorized into two main types [19]:

Type I (SC I), also known as a Hard-Switching Fault (HSF), where the short-circuit condition exists before the device is turned on.

Type II (SC II), also known as a Fault Under Load (FUL), where the device is already in the on-state when the short-circuit occurs.

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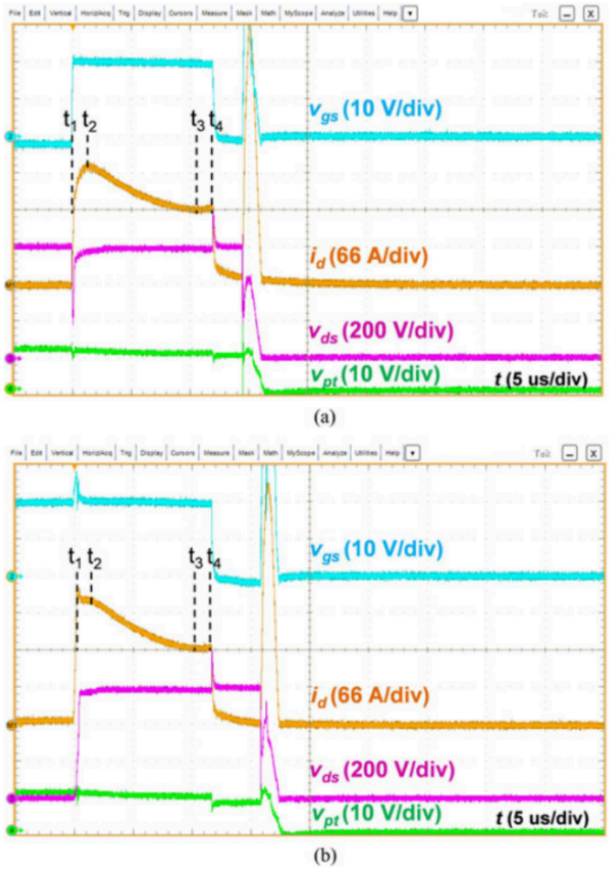

Figure 3. Typical short-circuit waveforms of a SiC MOSFET. Experimental waveforms for a 1200 V SiC MOSFET showing the drain current (id), drain-source voltage (vds), and gate-source voltage (vgs) under (a) Hard-Switching Fault (HSF) and (b) Fault-Under-Load (FUL) conditions. The four distinct stages of the SC event (t1 to t4) are illustrated, showing the initial current peak followed by a decrease due to self-heating. (Adopted from [4])

During a typical SC event, the drain current (I_d) rapidly increases to a peak value. Following this peak, the current begins to decrease due to device self-heating, which reduces carrier mobility in the MOS channel and drift region [20] (See Fig. 3). In some cases, as the junction temperature continues to rise, the drain current may begin to increase again just before failure [4]. This secondary rise is attributed to the leakage current increasing at a faster rate than the channel current is decreasing.

Experimental studies have identified two distinct failure modes under these conditions [20,21]:

Failure Mode I (Gate Failure): In this mode, the device fails due to a short between the gate and source terminals, but the drain-source pn-junction remains capable of blocking voltage. This mode is often associated with the breakdown of the gate's interlayer dielectric and is more prevalent under higher gate drive voltages.

Failure Mode II (Thermal Runaway): This failure mode results in all three terminals of the MOSFET (gate, drain, and source) becoming shorted. This catastrophic failure is typically driven by thermal runaway and is more commonly triggered by high DC bus voltages.

The behavior under SC II (FUL) conditions in SiC MOSFETs shows notable differences from that in Si IGBTs. While IGBTs exhibit a much larger current peak during SC II compared to SC I, the difference is less pronounced in SiC MOSFETs. This distinction is largely due to the much smaller Miller capacitance (C_{GD}) in SiC MOSFETs. Simulations show that increasing a SiC

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MOSFET's C_{GD} causes a larger gate voltage overshoot and results in SC II behavior that more closely resembles that of an IGBT, with a significantly higher and sharper current peak. Furthermore, under SC II conditions, a larger gate resistance (R_G) can paradoxically lead to a higher peak short-circuit current, as the rapid change in drain-source voltage induces a larger displacement current through the Miller capacitance, causing a more severe overshoot on the gate voltage [19].

The short-circuit withstand time (SCWT) is a critical parameter and is strongly influenced by operating conditions. The SCWT decreases significantly with an increase in DC bus voltage [20] and case temperature [4]. However, SCWT appears to be largely independent of the die size. While the critical energy (E_{SC}) to failure has a linear dependence on the active chip area, the SCWT remains almost constant because the increased thermal resistance of smaller chips counteracts the benefit of their lower SC saturation current [20].

2.3. Short-circuit failure mechanism of the SiC MOSFETs

The physical mechanisms responsible for SC failures in SiC MOSFETs are rooted in the extreme electrothermal stress experienced by the device. The two primary mechanisms are thermal runaway and the breakdown of the gate dielectric structure [20,21].

Thermal Runaway: During a short circuit, immense power dissipation occurs within the device, leading to a rapid rise in the internal junction temperature [4]. TCAD simulations consistently show that the temperature peak is localized in the JFET region of the device structure [22]. This extreme heat creates a positive feedback loop on the intrinsic carrier density, causing a dramatic increase in leakage currents, with the thermal generation component being dominant [4]. This high leakage current can be sufficient to activate the parasitic Bipolar Junction Transistor (BJT) inherent in the MOSFET structure, triggering an uncontrollable rise in current that leads to device destruction. This failure often manifests as a "delayed failure," where the device is successfully turned off, but a remaining tail leakage current leads to thermal runaway after a short delay.

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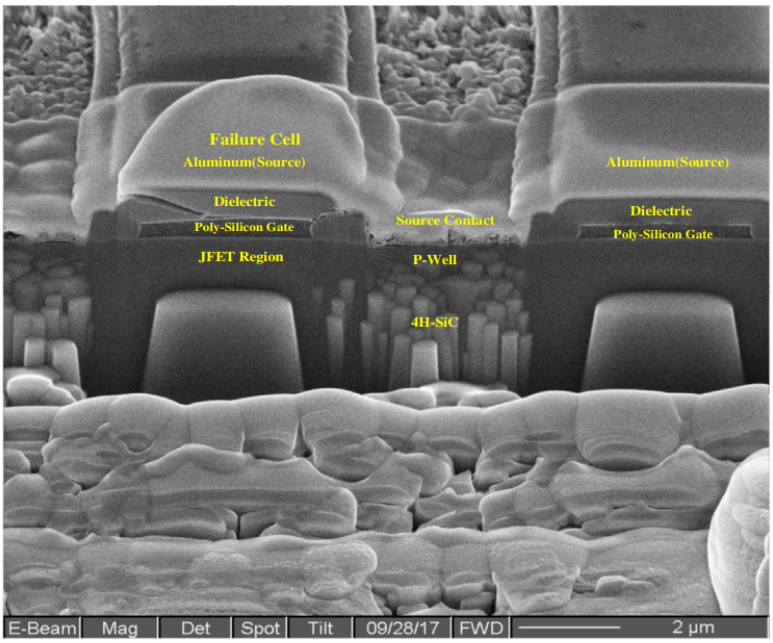

Figure 4. Microscopic View of Gate Dielectric Breakdown. Cross-sectional SEM image of a failed SiC MOSFET cell after a short-circuit event. The image, obtained after Focused Ion Beam (FIB) cutting, shows a damaged cell (left) next to a normal cell (right). Note the deformation of the aluminum and polysilicon layers and the cracks in the interlayer dielectric, which are caused by thermomechanical stress. (Adopted from [20])

Gate Interlayer Dielectric Breakdown: This mechanism is the physical origin of Failure Mode I and is driven by thermomechanical stress [20]. Microscopic failure analysis through Scanning Electron Microscopy (SEM) and Focused Ion Beam (FIB) cutting reveals significant structural damage(See Fig. 4). This includes obvious deformation of the aluminum source metal and polysilicon gate layers, accompanied by cracks that propagate through the interlayer dielectric (SiO_2) separating them [21]. At sufficiently high temperatures, the aluminum metallization can melt and diffuse into these cracks, creating a permanent short between the gate and source. The fundamental cause of this stress is the large mismatch in the coefficient of thermal expansion (CTE) between the source aluminum layer (23.2×10^{-6}/K), the gate polysilicon (2.9×10^{-6}/K), and the interlayer SiO_2 dielectric (0.5×10^{-6}/K). It has also been proposed that the mechanical failure of the SiO_2 ILD can occur at temperatures around 600 K, which is below the melting point of aluminum (933K). This suggests that even without melting, the thermomechanical stress can be high enough to form cracks into which the aluminum can be forced, leading to failure [21]. The "Lucky Defect Model" further posits that extrinsic, pre-existing point defects within the gate oxide can act as localized current pathways via trap-assisted tunneling, creating hotspots that accelerate this breakdown process [23].

3. Short-circuit protection and detection methods

Due to the weak short-circuit withstand capability of SiC MOSFETs, which is a result of their smaller chip area and higher current density, a fast and reliable short-circuit protection (SCP) function is critical for any system employing these devices. The required protection time for SiC MOSFETs is significantly shorter than for Si IGBTs, typically needing to be within 2-3 microseconds, compared to the 10 microseconds for IGBTs [24]. An effective SCP system is

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composed of two essential stages: first, the rapid detection of the short-circuit event, and second, the safe turn-off of the device to prevent catastrophic failure.

3.1. Short-circuit detection methods

The detection of a short-circuit event must be accomplished in the shortest possible time to minimize damage. Various methods have been developed, which can be categorized based on the electrical parameter being monitored: drain-source voltage (V_{DS}), drain-source current (I_{DS}), or gate-related characteristics [25]. This paper introduces 4 categories of detection methods.

3.1.1. VDS-based detection methods

Desaturation (De-sat) Detection(See Fig. 5): This is the most common method in engineering due to its simplicity and reliability. It works by monitoring the $V_{DS}$of the MOSFET during the on-state. Under normal operation, $V_{DS}$is low, but during a short circuit, it rises significantly, exceeding a preset threshold and triggering the protection circuit. The main drawbacks of this method are its relatively long detection delay (450ns to 1.5µs) and its susceptibility to false triggers, particularly as the on-state voltage of SiC MOSFETs is highly sensitive to temperature changes. To shorten the delay, parameters such as the blanking capacitor and associated resistors must be carefully optimized.

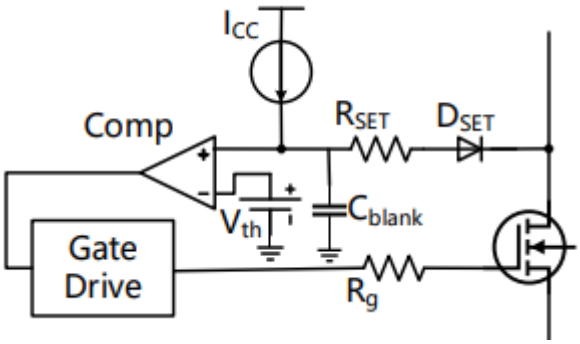

Figure 5. Desaturation Detection circuit. A simplified circuit diagram of the conventional desaturation detection method. The circuit monitors the drain-source voltage (VDS) and triggers a fault via the comparator (Comp) when it rises above a predefined threshold, indicating a short-circuit condition. (Adopted from [25])

dVds/dt Detection: This method monitors the rate of change of the drain-source voltage. A short-circuit causes a very rapid increase in V_{DS}, and this high dv/dt is detected by a high-speed comparator. This approach is fast, with response times around 250ns, but it is generally only effective for Hard-Switching Faults (HSF) and has low noise immunity.

3.1.2. IDS-based detection methods

Rogowski Coil: This non-intrusive method uses a PCB-integrated Rogowski coil to measure the rate of change of the drain current (di/dt) and obtains the current value through an integrator circuit. It is extremely fast (response time <100 ns), has high noise immunity, and is effective for both HSF and Faults-Under-Load (FUL). However, the circuit design is complex and can be costly.

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dIds/dt Detection (Source Inductance): This technique measures the voltage across a small parasitic or intentionally added inductance in the source path to infer the di/dt. While fast (<100ns) and moderately complex, it can be inconsistent in FUL scenarios, often requiring different thresholds for HSF and FUL detection.

Tunnel Magnetoresistance (TMR) Sensor: TMR sensors detect the change in the magnetic field produced by the high short-circuit current. This method offers high sensitivity, fast response (<100ns), and strong resistance to electromagnetic interference, but comes at a high cost and design complexity.

3.1.3. Gate-based detection methods

Gate Charge (Q_G) Monitoring: This technique leverages the fact that during an HSF, the characteristic Miller plateau in the gate charge curve disappears because the drain-source voltage remains high. This results in a total gate charge (Q_{sc}) that is significantly lower than during normal turn-on [24]. By comparing the measured gate charge against a reference value, a short circuit can be detected quickly (~173ns) [25]. Its main limitation is that it is only effective for HSFs and can be sensitive to noise and temperature.

Combined Detection Methods

VGS and dI_{ds}/dt Detection: This two-dimensional approach simultaneously monitors both the gate-source voltage and the drain current's rate of change. By comparing these two parameters against predefined thresholds, it can identify faults with extreme speed (HSF <50ns, FUL <100ns) and high sensitivity. However, the circuitry is complex and requires precise calibration [25].

3.2. Soft Turn-Off (STO) strategies

Once a short circuit is detected, the MOSFET must be turned off safely. An abrupt turn-off would cause the high short-circuit current to change instantaneously, inducing a dangerously large voltage spike across the circuit's parasitic inductances ($V=L\cdot di/dt$). This voltage spike can easily exceed the device's breakdown voltage, leading to catastrophic failure. Soft Turn-Off (STO) strategies are therefore employed to gradually reduce the gate voltage, which in turn allows the drain current to decrease in a controlled manner, minimizing voltage overshoot, EMI, and thermal stress [25].

Soft Slope Turn-Off: This method uses an additional resistor (R_{soft}) and a sinking MOSFET to create a controlled, gradual discharge path for the gate. This smoothly reduces the gate voltage, resulting in a gentle current ramp-down. While simple in design, it has a slower response time (~900ns) and must be customized for different SiC MOSFETs due to variations in their input capacitance (C_{GS}).

Two-Step Turn-Off: This approach uses a Zener diode and a sinking MOSFET to turn the device off in two stages. First, the gate voltage is clamped to an intermediate level, allowing the drain current to decrease partially. This is followed by a complete turn-off by the main driver. This method offers a good balance between switching speed and voltage spike suppression, with a response time of around 500 ns, and is less dependent on the specific device being used. Its primary drawback is the potential to create two smaller V_{DS} spikes during the process.

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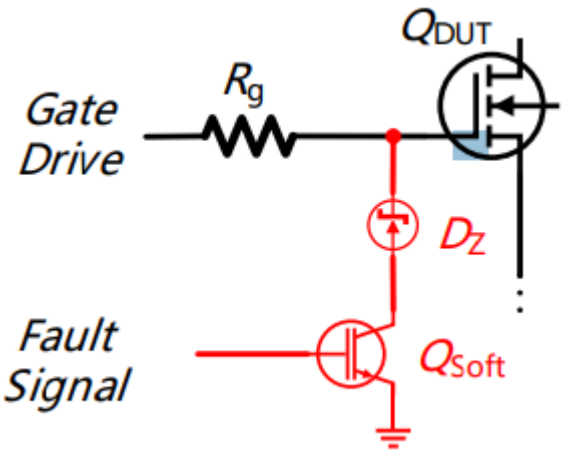

Figure 6. Two-Step Soft Turn-Off (STO) Circuit. The circuit topology for the Two-Step STO strategy. Upon receiving a fault signal, the sinking MOSFET (Qsoft) and Zener diode (DZ) first clamp the gate voltage to an intermediate level to begin a controlled current reduction, after which the main gate driver fully turns off the device. (Adopted from [25])

Multi-Step Turn-Off (MSTO): This is the most advanced and complex strategy, utilizing a digitally controlled array of MOSFETs to dynamically adjust the gate discharge current in real-time. By continuously sensing the VDS variation, the controller can precisely manage the turn-off process to minimize voltage spikes and EMI. While offering superior protection and control, it has the highest complexity, cost, and a wide range of response times (166ns to 1642ns) [25].

4. Conclusions

This paper has provided a comprehensive review of the critical reliability challenges facing SiC MOSFETs under short-circuit conditions, synthesizing findings on their failure mechanisms and corresponding protection strategies. The investigation confirms that the limited short-circuit withstand capability of SiC MOSFETs is an inherent consequence of their design for superior performance, primarily driven by rapid thermal stress that leads to two distinct failure modes: gate interlayer dielectric breakdown and catastrophic thermal runaway. Furthermore, the analysis of protection methodologies reveals a crucial trade-off between the simplicity of conventional techniques, such as desaturation detection, and the ultra-fast response required to safeguard these sensitive devices. Advanced methods that monitor current directly or combine multiple parameters offer the necessary sub-microsecond detection speeds but at the cost of increased system complexity. Critically, this review establishes that effective fault detection must be coupled with a robust Soft Turn-Off (STO) strategy to manage and suppress destructive voltage overshoots, which is an indispensable component of a complete protection scheme. Ultimately, ensuring the reliable operation of SiC MOSFETs demands a holistic approach that integrates an understanding of the underlying physical failure mechanisms with the design of sophisticated, fast-acting, and complete protection circuits.

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