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108Bc/Hz@1MHz 255MHz Voltage-controlled Dual-Ring Oscillator Simulation Design

Hanfei Yue

Wang Zheng College of Microelectronics, Changzhou University, Changzhou, China
483679634@qq.com

Abstract. This paper presents a voltage-controlled dual-ring oscillator (VCDRO) with low phase noise and a wide tuning range, implemented in TSMC 65 nm CMOS technology. Low-noise inverters are used as the delay cells for the rings. Simulations were performed in Cadence Virtuoso. Under a tuning voltage range of 0.5 V to 1.2 V the oscillator tunes from 83 MHz to 255 MHz. At the 255 MHz operating point the phase noise is −85.1 dBc/Hz at 100 kHz offset and −108.0 dBc/Hz at 1 MHz offset. The RMS current is 286 μA.

Keywords: dual-ring, voltage-controlled oscillator (VCO), phase noise, TSMC 65 nm

1. Introduction

High-performance frequency sources play a decisive role in modern wireless communication systems (such as 5G/6G base stations), phased-array radar, and high-speed data converters; their phase-noise performance directly affects system spectral purity and bit-error rate [1–2]. For the sub-1 GHz band—serving as a core frequency range for high-speed SerDes interfaces and satellite intermediate-frequency local oscillators—stringent phase-noise requirements are imposed, with performance at 1 MHz offset expected to be better than −105 dBc/Hz. However, conventional single-ring voltage-controlled oscillators face significant challenges in achieving performance above −100 dBc/Hz at 1 MHz offset in the sub-1 GHz range, due to the up-conversion effect of active-device 1/f noise, the limited quality factor of the resonator (typically Q < 15), and additional phase noise introduced by tuning nonlinearity. These factors have become a key bottleneck restricting the development of high-precision systems.

To address this, this paper proposes an innovative VCO architecture based on coupled dual-ring loops. The scheme uses two parallel ring resonators; by exploiting phase anti-correlation it suppresses 1/f noise up-conversion, and the coherent energy superposition of the two oscillator cores effectively increases the loop equivalent Q above 20 [2–4]. The design target is a breakthrough phase-noise figure of −108 dBc/Hz at 1 MHz offset around a 255 MHz center frequency. Using the 65 nm CMOS process, circuit simulations were built on the Cadence Spectre platform with a focus on optimizing transconductor biasing and loop delay. The results present a new paradigm for high-precision frequency synthesizer design.

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2. Circuit design

The schematic of the five-stage ring VCO is shown in Fig. 1. The oscillator frequency is determined by the total delay of the five delay cells. The oscillation period of an N-stage ring oscillator is determined by:

$$T = 10\tau_d \tag{1}$$

Where τd is the delay of one inverter stage. The delay of each inverter stage is jointly determined by its load capacitance $C_{load}$and its output current $I_{out.}$ Assuming the inverter switching (voltage swing) crosses at Vdd/2,

$$\tau_d \approx \frac{C_{load}V_{dd}}{2I_{out}} \tag{2}$$

Therefore, the oscillation frequency of a 5-stage ring VCO is:

$$f_0 = \frac{I_{out}}{5C_{load}V_{dd}} \tag{3}$$

which shows that the oscillation frequency is proportional to the delay-cell output current.

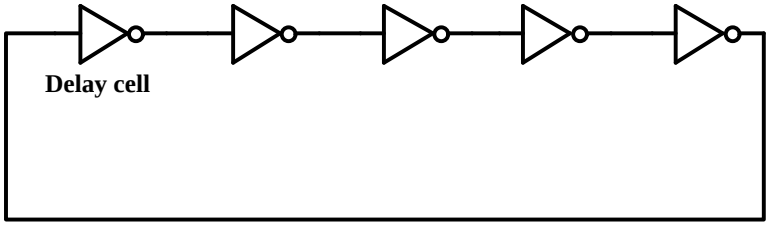

Figure 1. Five-stage ring oscillator

The delay cell used in this study is shown in Fig. 2. Based on a conventional inverter, a first-order filtering network composed of a resistor R and a capacitor C is introduced to reduce the output noise of the inverter. This approach does not increase additional current consumption, though it does require slightly more layout area. When designing the device parameters of the inverter, the output impedances of the PMOS and NMOS transistors should be made as consistent as possible to ensure that the switching voltage remains around Vdd/2. In this design, the PMOS has W/L=1.42 μm/800 nm, and the NMOS has W/L=300 nm/800 nm.

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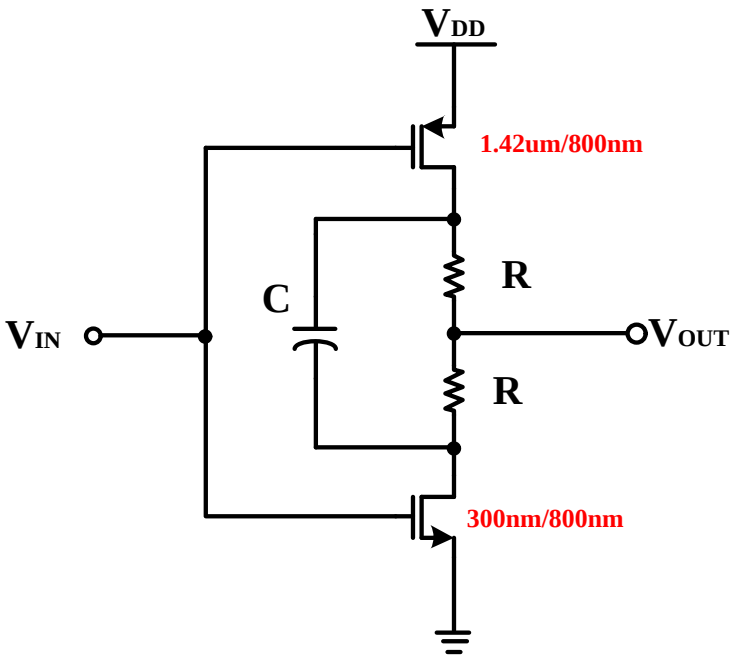

Figure 2. Delay cell

The proposed dual-ring oscillator topology is shown in Fig. 3. The tuning voltage Vt is connected to two parallel ring oscillators, enabling common tuning of both loops. Compared with a conventional single-ring VCO, the dual-ring VCO provides a 3 dB improvement in phase noise, making it more suitable for low-noise applications. A buffer stage ensures the oscillator output amplitude is sufficiently large [5].

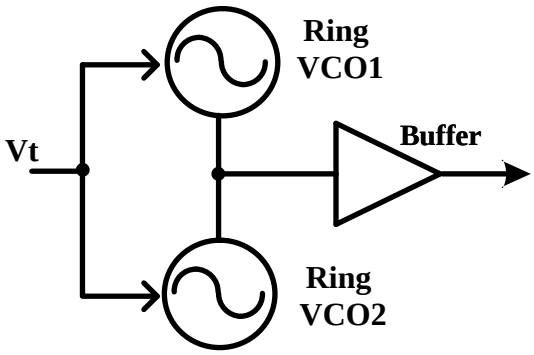

Figure 3. Proposed dual-ring oscillator

3. Simulation results

The dual-ring VCO was simulated in Cadence Virtuoso using TSMC 65 nm GP process models. Time-domain (tran), periodic steady-state (PSS), and phase-noise (PNoise) analyses were used to evaluate current consumption, phase noise, and tuning range. Simulation results are shown in Figs. 4–5.

The simulated tuning range is shown in Fig. 4. With tuning voltage Vt swept from 0.5 V to 1.2 V the oscillator tunes from 83 MHz to 255 MHz. The results also show good frequency tuning

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linearity: for every 100 mV increase in tuning voltage, the resonance frequency increases by approximately 24.5 MHz. This linearity benefits from the higher equivalent Q of the dual-ring filter.

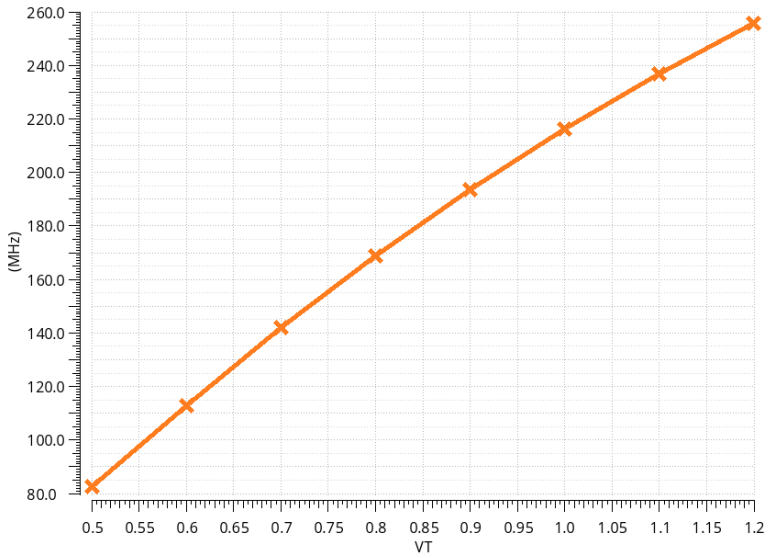

Figure 4. Tuning-range simulation result

Phase-noise simulation results are shown in Fig. 5. The phase noise is −85.1 dBc/Hz at 100 kHz offset, −108.0 dBc/Hz at 1 MHz offset, and −129.2 dBc/Hz at 10 MHz offset. The phase noise improvement from 100 kHz to 1 MHz is about 23 dB, and from 1 MHz to 10 MHz about 21 dB, which is attributed to the RC filtering within the delay cells that further reduces noise.

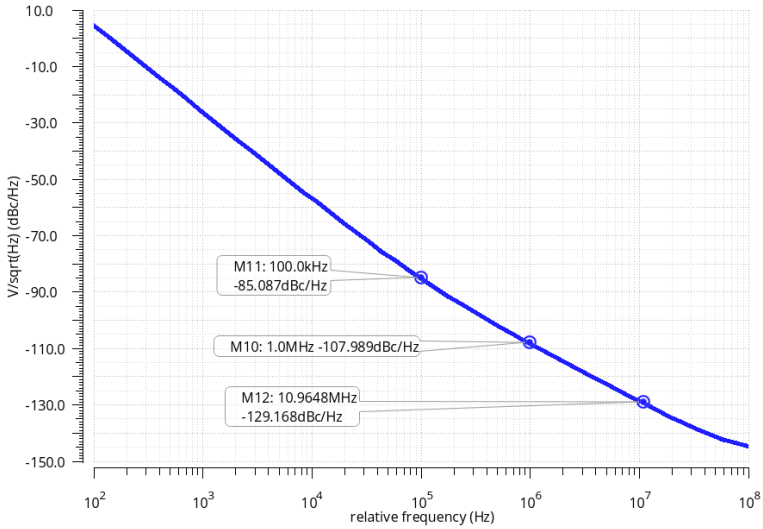

Figure 5. Phase-noise simulation result

4. Conclusion

This paper proposed a dual-ring VCO that uses low-noise inverters as delay cells. Compared with traditional ring VCOs, the proposed design achieves superior phase-noise performance. Simulations demonstrate a tuning range of 83 MHz–255 MHz for a tuning voltage of 0.5 V–1.2 V. The measured

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phase noise is −85.1 dBc/Hz at 100 kHz offset, −108.0 dBc/Hz at 1 MHz offset, and −129.2 dBc/Hz at 10 MHz offset. At 255 MHz the RMS current is 286 μA.

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