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Self-Heating Effect of Gate-All-Around FETs: A Review

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Abstract: As MOSFETs evolve into gate-all-around field effect transistor (GAAFET), the impact affecting the performance of MOSFET becomes more significant: the temperature rise caused by self-heating effect (SHE). This review paper presents the development process of field effect transistors (FET), from Planar FET to GAAFET, including their SHE. It introduces the formation mechanism of SHE, and compares the temperature distribution of different FETs under the influence of SHE and the performance of various FET structures in terms of heat conduction and dissipation. Three harmful factors for FET caused by SHE is discussed, including bias temperature instability (BTI), hot carrier injection (HCI), and electromigration (EM). These factors accelerate the aging mechanism of all kinds of FETs. As for GAAFET, the main influencing factors of its aging are BTI and EM. The paper concludes by reviewing current solutions to mitigate SHE-induced temperature rise and offers insights and recommendations for future research.

Keywords: FinFET, gate-all-around FET, self-heating effect, nanowire (NW), heat dissipation

1. Introduction

The integrated circuits industry largely depends on semiconductor devices, among which the most critical components are MOSFETs. As the foundation of integrated circuits, MOSFETs have continuously evolved in pursuit of smaller sizes and higher performance through successive technological innovations. From Planar FET to FinFET, and now to GAAFET, the size of transistors has been continuously reduced and the performance of integrated circuits has been greatly improved.

Planar FET pioneered the use of planar gates to control channel current via the field effect, significantly reducing chip size. However, due to its planar structure and short-channel effects, further reduction of device size is limited. FinFET introduced a fin-like 3D gate structure, enhancing gate control over the channel, improving circuit precision, and reducing leakage current [1]. This further reduces the size of the chip and improves its performance. While FinFET remains widely used, its scalability is challenged by the 7nm size limit imposed by current technologies [2].

To break this limit, many manufacturers including SAMSUNG have started to explore the practicability of GAAFET process. GAAFET advances beyond FinFET with its surrounding gate structure, offering superior control over channel current and enhanced transistor performance. However, the commercialization of GAAFET still faces some obstacles.

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Apart from low yield caused by production processes, the more obvious temperature rise GAAFET faces also needs to be urgently solved. The heat generated by current flow between source and drain can't be removed due to poor thermal conductance, leading to temperature rise of device. This is known as the self-heating effect [3].

While SHE affects various MOSFETs, its impact on GAAFET temperature is particularly severe due to GAAFET's unique structure. The significant temperature rise of GAAFET leads to considerable device degradation, including performance degradation and lifetime reduction.

This device degradation increases the cost of applying integrated circuits based on GAAFET, hindering the development of integrated circuits industry and posing a significant barrier to the advancement of the semiconductor industry. To address this issue, this article will compare SHE across various FET types, examine its impact on GAAFET, review existing mitigation strategies, and offer insights and recommendations for future research.

2. From FinFET to GAAFET

In the history of MOSFET development, researchers are constantly trying to scaling the FETs. For the semiconductor industry, smaller transistor means that electronic devices of the same volume can carry more transistors. This will reduce the size or increasing the capacity of electronic devices. Even though doing so may increase the production costs, it is still a trend in the development of the electronics industry. Following this trend, there are two very important innovation nodes of MOSFET: FinFET and GAAFET.

FinFET is a self-aligned double-gate MOSFET, named for its unique fin-shaped silicon body structure shown in Fig.1(a). The silicon body is thin and vertical, surrounded by gates on both two sides and the top, forming a three-sided gate control [1,4,5,6]. FinFET effectively suppresses the short channel effect [7], enhances the control capability of the device and allows more precise threshold voltage control [8]. It is manufactured using quasi-planar technology [9], which is relatively easy to integrate into existing processes, supports further scaling, and is suitable for advanced integrated circuit manufacturing.

GAAFET is a silicon-on-insulator transistor as shown in Fig.1(b) with a fully surrounding gate [10,11]. Its core feature is that the active silicon film is completely surrounded by a thin gate oxide and polysilicon gate, including the top, bottom and sides, forming all-round gate control [12]. This design not only enhances the control capability of the transistor, but also effectively reduces the short-channel effect [13], improves switching speed and energy efficiency. The manufacturing process of GAAFET is relatively simple, and only a small number of steps need to be added to the standard SOI process to achieve better electrical characteristics and better scalability.

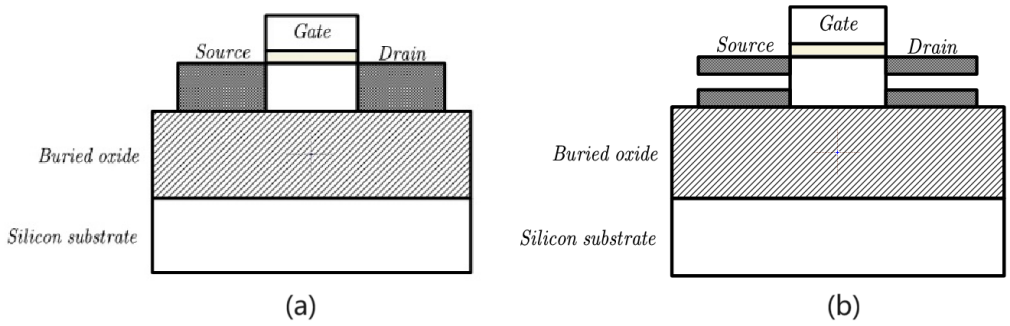


Figure 1: Conventional thin-film SOI FinFET (a) and GAAFET (b)

Although both FinFET and GAAFET use a wrap-around gate design to enhance the control capability of transistors, they still have differences in structure. FinFET is characterized by its

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vertical silicon fin structure, with the gate wrapped around three sides of the silicon fin, which is suitable for high-density integration and effectively controls the short channel effect [7]. GAAFET, on the other hand, achieves a fully wrapped gate layout by forming a gate on the entire surface of the silicon film (including the top and bottom) [10]. This structure directly increases the contact area between the gate and the silicon film, thereby better controlling the current in the transistor and further reducing the size of the transistor even when affected by the short channel effect. In short, FinFET is characterized by a vertical fin structure and a three-sided gate wrap-around, while GAAFET is characterized by a full-surface gate wrap-around.

GAAFET is designed to break through the 7nm [2] volume node of transistors, so all improvements are based on how to effectively suppress the short channel effect. By splitting the fin-shaped protrusion gate with only three contact surfaces into an independent gate fully wrapped on four sides, the contact area between the GAAFET silicon film and the gate are greatly increased. This change better controlling the flow of current in the transistor and avoiding the breakdown of the gate due to the close distance between the source and the drain in the process of further scaling the transistor. However, the design of splitting the gate to pursue a larger contact area also brings negative effects: more serious heat generation than other FETs and lower production yield. Due to the increase of the production yield is mainly based on improvement of the production process, this paper mainly discusses the heat generation in GAAFET. The phenomenon of heating itself inside the FETs is called the self-heating effect.

3. Self-heating effect

Self-heating effects have been an unavoidable problem from the invention of FETs. Especially in the process of continuous improvement and scaling of FETs, the self-heating effect is becoming more and more serious, which strongly affects the performance of the device. Therefore, it is necessary to fully study the self-heating effect.

3.1. The Formation mechanism of the Self-heating effect

The self-heating effect in FETs is mainly due to the Joule heating accumulation that occurs when the current between the source and drain passes through the channel in the conduction state of the FET, resulting in an increase in the temperature of the device. The main factors of the self-heating effect are the high current density of FETs when they are forward biased, the low thermal conductivity of semiconductor materials and oxide insulator materials, and the difficulty of heat removal due to the structure of FETs.

The mechanism of the self-heating effect is that in the conduction channel controlled by the gate, the high-energy electrons will scatter with the phonons that cause the lattice to heat up, thereby reducing the mobility of the carriers and thus reducing the average phonon mean free path [14]. At the same time, FET devices have a high transistor density and dissipate a lot of heat per unit area. In the case of Planar FETs, due to the two-dimensional planar structure of the gate and the large channel width, they have a large heat dissipation area that can dissipate heat through the Si substrate more quickly, so we will mainly discuss the self-heating effects of FinFETs and GAAFET here.

For more advanced FinFETs and GAAFETS, the size of the fins and silicon nanowires is similar to or even smaller than the average phonon mean free path, resulting in increased phonon boundary scattering and increased device thermal resistance, which results in a 10X reduction in the thermal conductivity of silicon in fins and 25X in silicon nanowires [15]. Especially for GAAFET, the size of silicon nanowires is smaller than the fins of FinFETs, which makes the phonon boundary scattering stronger. This greatly exacerbates the self-heating effect. In addition, the number of fins/silicon nanowires in FinFETs and GAAFETS also significantly affects the self-heating effect.

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As shown in Fig.2, the average temperature of the device increases significantly as the number of fins/nanowires increases.

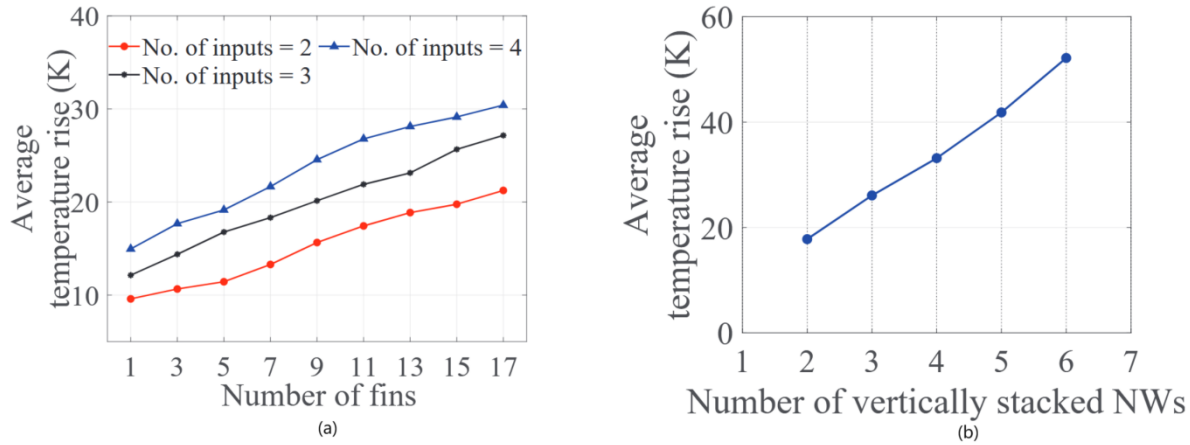


Figure 2: (a)The average temperature of FinFETs at saturation increases with the number of fins.Different colored lines represent different input voltages. (b)The average temperature of GAAFETs at saturation increases with the number of silicon nanowires [14]

3.2. Temperature distribution in FinFET and GAAFET

For general MOSFET devices, the rate of heat generation H(W/m^3) of the channel lattice is calculated by the formula:

$$H = \vec{J} \cdot \vec{E} \tag{1}$$

Where is the current density and is the electric field strength [14]. Since the electric field in the channel is concentrated in the drain and its extended region when the MOSFET is operating, it can be seen from (1) that the heat generation and temperature are highest at the drain and its extended region [16,17]. Fig.3 illustrates the distribution of the heating rate H at different locations in the channel, and it can be seen that the heating reaches its peak in the drain and its extension area.

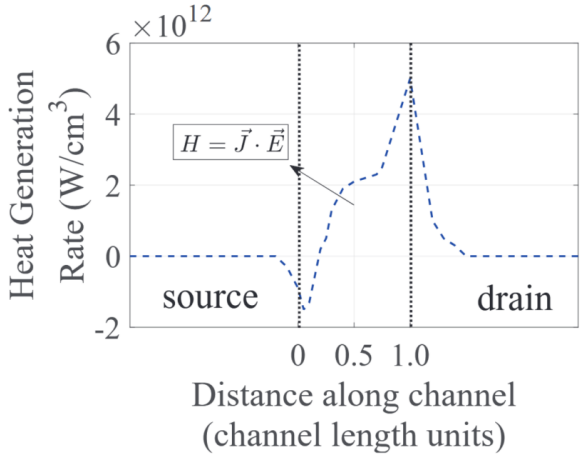


Figure 3: Distribution of heating generation rate in the direction of the extension channel [14]

In FinFETs, Fig.4 shows that the steady-state operating temperature is mainly distributed in the fins, gates, and drains and their extension regions.

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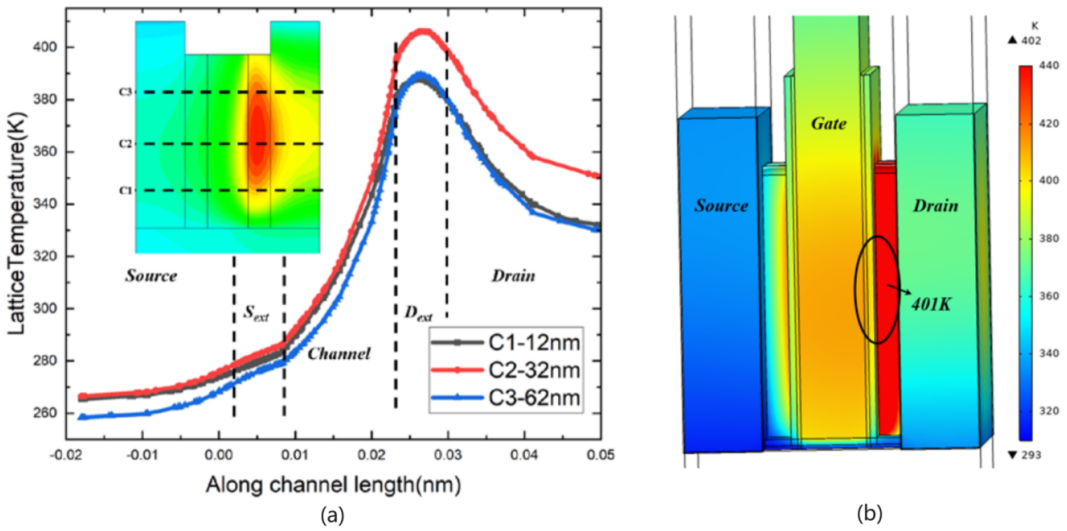


Figure 4: (a)The main temperature distribution area of FinFET when it is saturated. (b)Stereo Diagram of FinFET temperature distribution in saturated operation [18]

In GAAFET, it can be seen from Fig.5 that the steadystate operating temperature is mainly distributed in the silicon nanowires, gates, and drains and their extension regions.

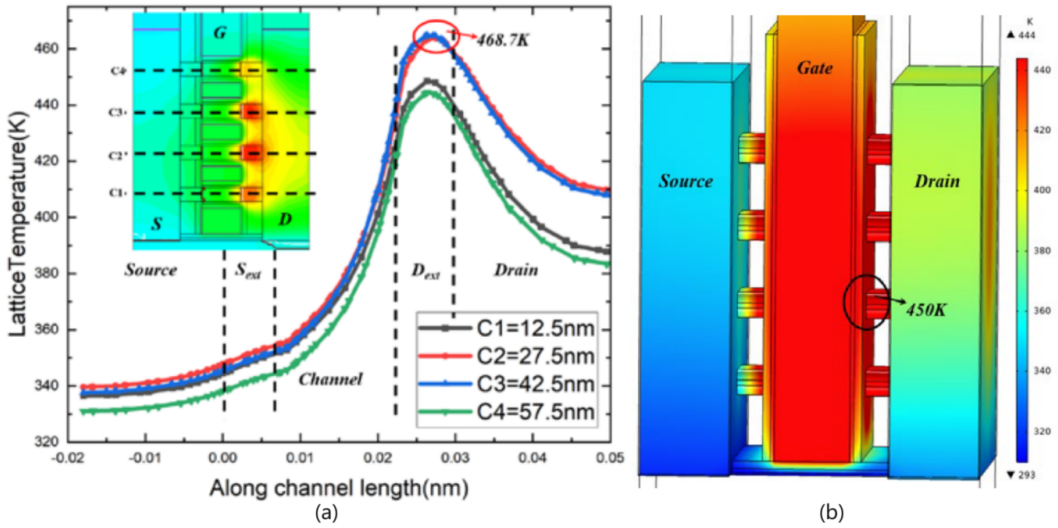


Figure 5: (a)The main temperature distribution area of GAAFET during saturation operation. (b)Stereo diagram of GAAFET temperature distribution in saturated operation [18]

3.3. Heat conduction paths in FinFET and GAAFET

In general,the heat generated by the drain and its extended area after the forward biased MOSFET is mainly conducted by two ways. One is going upward along the channel and gate through the metal contacts and connections. Another is going downward through the oxide insulation and substrate to the substrate.

For FinFETs, the heat generated by the drain and its extended area first reaches the channel, then to the gate, and finally down to the oxide insulation and substrate. The heat transfer path of the FinFET can be seen in Fig.6, which shows the time point at which the heat reaches the channel, gate, and substrate from the beginning of heat production.

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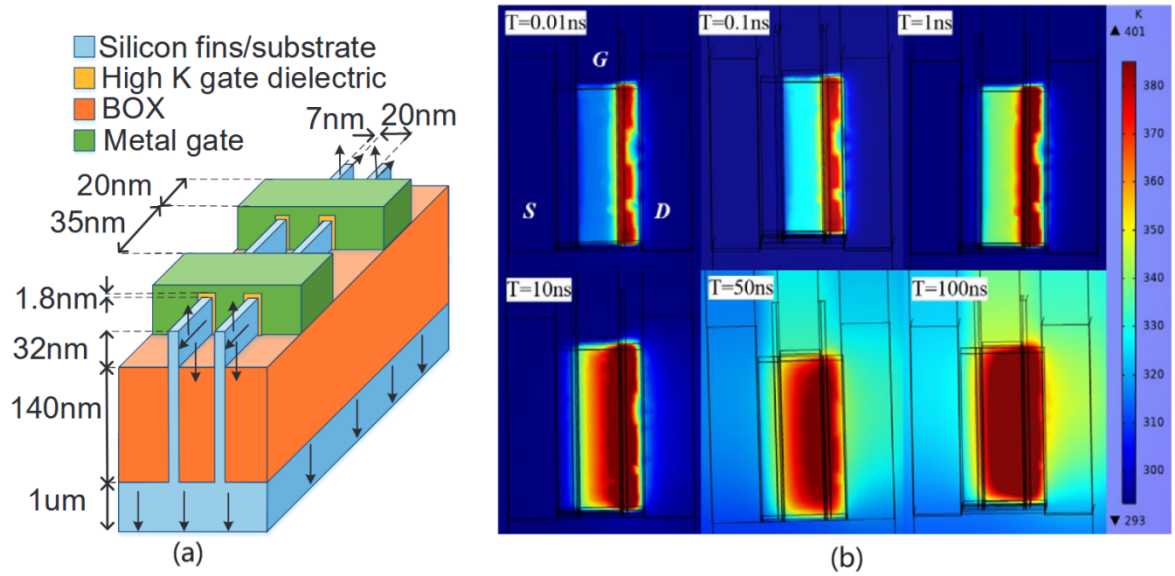


Figure 6: (a) Heat conduction path in FinFET, arrows indicate heat transfer direction.[14] (b) The point in time when FinFETs start heating up and reach the channel, gate, and substrate [18]

For GAAFET, the heat generated by the drain and its extension area first reaches the channel, then to the gate, and finally down to the ox ide insulation and substrate. However, because the silicon nanowires in GAAFET are surrounded by an oxide insulating layer, the heat generated by the drain extension region is more difficult to conduct through the substrate than that of FinFETs, so GAAFET has a more serious self-heating effect than FinFETs. The heat transfer path of the FinFET can be seen in Fig.7, which shows the time point at which the heat reaches the channel, gate, and substrate from the beginning of heat production.

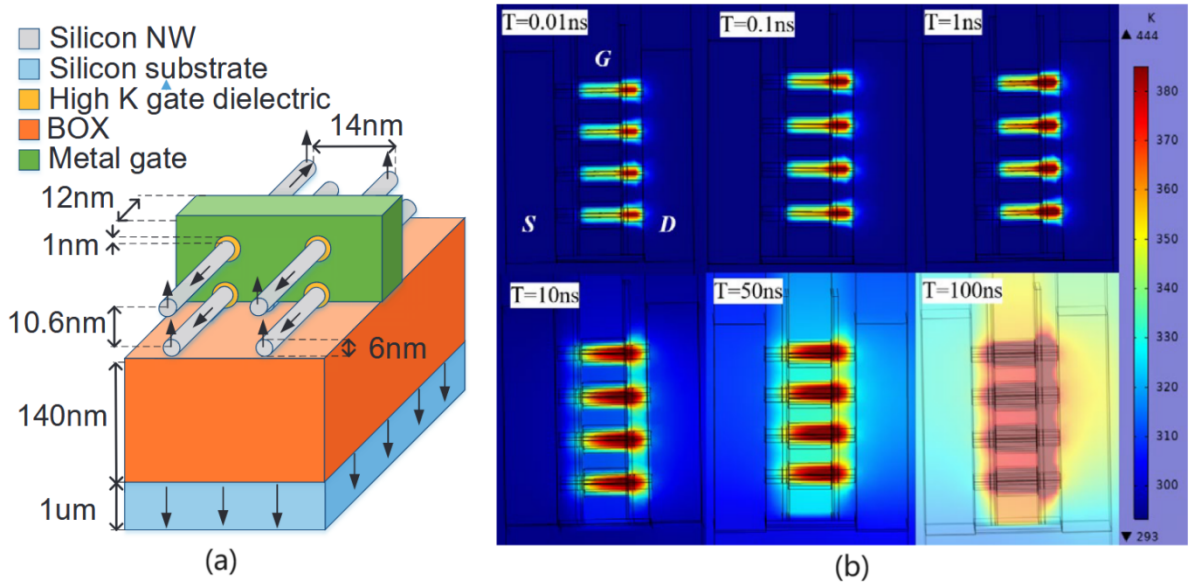


Figure 7: (a) Heat conduction path in GAAFET, arrows indicating heat transfer direction.[14] (b) The time point at which GAAFET starts with heat generation and reaches the channel, gate, and substrate [18]

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4. Impact of SHE on device

The impact of SHE on the reliability of transistors is mainly reflected in three aspects: BTI, HCI and EM. These three phenomena all lead to device degradation and can be accelerated by the temperature rise caused by SHE.

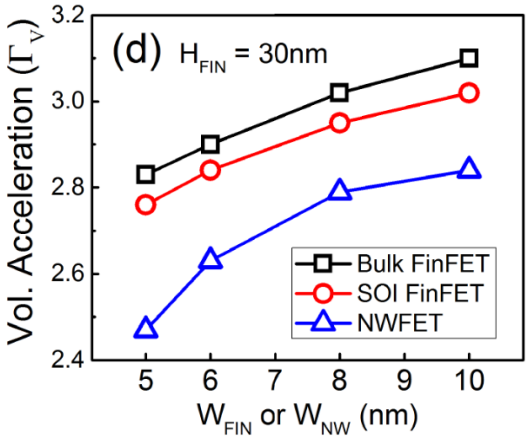


Figure 8: W_{FIN} and W_{NW} dependence of NBTI voltage acceleration factor for FinFETs and NWFETs [19]

The degree of BTI degradation is intensified by two factors: the scaling of FET and the temperature rise. As shown in Fig.8, under the same voltage stress conditions, the voltage acceleration factor of nanowire FET is smaller than that of FinFET, and it drops more as the device size decreases [19]. This result suggests that BTI increases when device size decreases, leading to higher device degradation. This also means that compared to FinFET with a fin-shaped structure, BTI is more obvious in GAAFET with a nanowire structure, resulting in more severe device lifetime shortening.

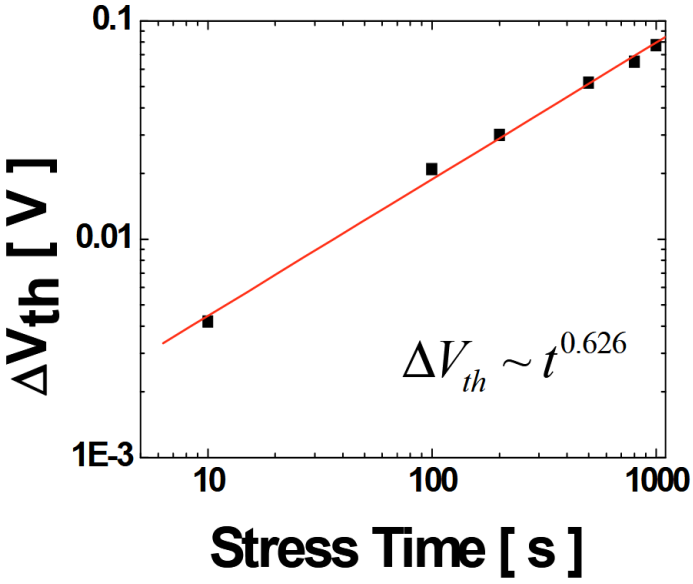


Figure 9: The degradation of threshold voltage (ΔV_{th}) with stress time [21]

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In heavily doped substrates, the temperature rise caused by SHE increases the carrier mobility. This reduces the energy required for hot carrier injection into the gate oxide, making HCI easier to occur [20]. Fig.9 shows the relationship between threshold voltage and stress time, indicating that HCI can cause degradation of threshold voltage, which leads to device performance degradation [21]. However, HCI does not very depend on temperature [22], but is affected more by stress time and substrate doping levels [20]. Therefore, the impact of SHE on the reliability of HCI may not be a critical issue.

EM is a failure mechanism of electronic components that can be accelerated by high temperature. When the electrons in the current collide with metal atoms in the semiconductor, the metal atoms migrate and leave voids [23]. As the metal atoms continue to migrate, the resistance of the semiconductor increases, causing degradation of device performance. The temperature rise caused by SHE increases carrier mobility, making EM more severe. This phenomenon leads to a reduction of time to failure of the device.

In Planar FET and FinFET, BTI, HCI, and EM cause different forms of device degradation. With the reduction of device size and the increase of operating temperature, device aging caused by wear out is accelerated. This not only means the reduction of device lifetime but also means that wear out will lead to a decrease in device performance over time [24].

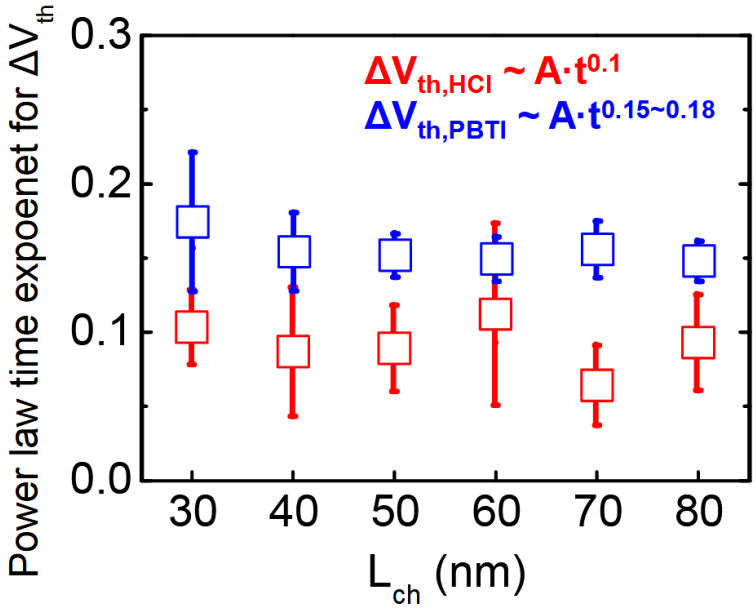


Figure 10: Power law time exponent of ΔV_{th} depending on channel length extracted from ΔV_{th} [25]

In GAAFET, the degradation mechanism and effect of BTI are similar to that in FinFET. Due to the low thermal conductivity of the nanowire structure, the more significant temperature rise and thermal coupling effect make EM have a greater impact on GAAFET degradation. However, HCI does not have a significant impact on the degradation of GAAFET. As shown in Fig.10, the time exponent of HCI is only about 0.1, which is considerably smaller than BTI's 0.15 to 0.18[25]. This indicates that HCI does not contribute much to the reduction of time to failure of GAAFET, and that BTI and EM dominate the degradation of GAAFET [14].

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5. Possible solutions to SHE

As the size of MOSFETs continues to shrink, the impact of self-heating effects is also increasing. In order to effectively put GAAFETs into production use, we need solutions to address or mitigate the self-heating effects. To this end, we propose three solutions.

5.1. Use materials with higher thermal conductivity

The primary mechanism of self-heating effects is the reduction in material thermal conductivity caused by phonon boundary scattering. Therefore, we can design FETs using semiconductor materials and interconnect materials with higher thermal conductivity.

5.2. Alter the duty cycle of the current

Since the heat source of self-heating effects is the current, under the alternating current operation mode of GAAFETs, by changing the ratio of pulse time to off time—also known as the duty cycle—self-heating effects can be effectively suppressed. Under the premise of keeping the current operating frequency constant, a lower duty cycle can better suppress self-heating effects.

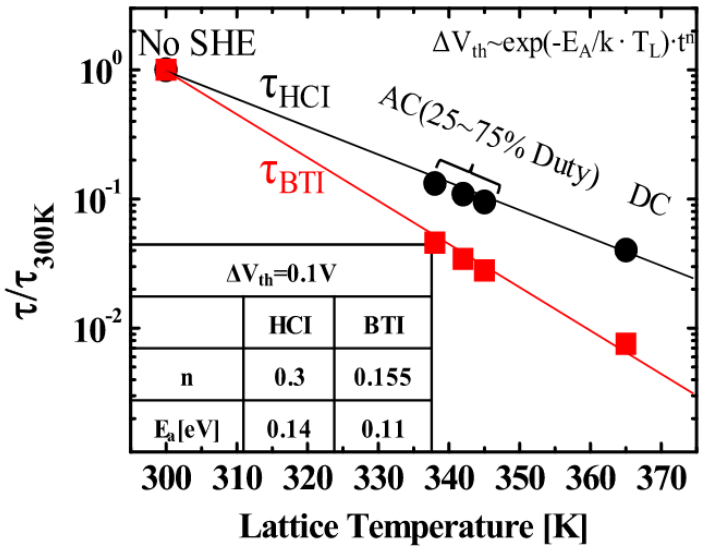


Figure 11: Comparison of HCI (black) and BTI (red) lifetime as a function of $T_{L,max}$. The $T_{L,max}$ is determined by SHE with the operation mode and for various duty cycles [26]

5.3. Increase air gap spacing and ambient gas pressure

Suppress self-heating effects by increasing the gap spacing within a certain range and the surrounding environmental gas pressure. The gap spacing and environmental gas pressure in FETs devices affect the thermal conductivity of the gas. The relationship is represented by the following formula:

$$\lambda_{gas} = \lambda_{p0}(1 + \frac{19(2-\zeta)\kappa_B T}{6\sqrt{2}\zeta p \delta_{gap}^3})^{-1} \quad (2)$$

Where δ_{gap} is the gate oxide gap, and λ_{p0} is the thermal conductivity of the gas at 1 atm [27]. Using (2), it's easy to calculate the relationship between the GAAFET gate oxide gap spacing and environmental gas pressure with the change in gas thermal conductivity [28], as is shown in Fig.12. This figure illustrates that within a certain range, increasing the gate oxide gap spacing and

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environmental gas pressure can significantly improve the thermal conductivity of the gas, thereby alleviating self-heating effects.

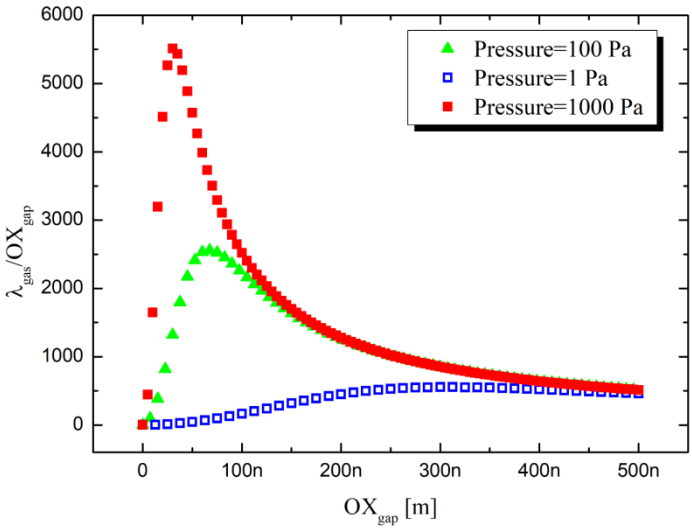


Figure 12: Variation of gas thermal conductivity with gate gap spacing and ambient gas pressure [28]

The above three solutions, from three different perspectives, reduce the self heating effect to different degrees by changing the transistor material, the current and the transistor operating environment. One of the most effective methods is to change the material of transistors and use semiconductor materials with high thermal conductivity. This can directly improve the thermal conductivity of transistors and reduce the temperature rise caused by self heating effect, but this method is more dependent on the study of high thermal conductivity materials in materials science. The easiest way is to change the duty cycle of the working current. This method can extend the heat radiation time of the transistor and alleviate the self heating effect. But the effect of this method is not very significant. The effect of the last method that changes the environmental gas pressure is between the effects of the other two methods. It is difficult to operate but has good results.

Therefore, in actual production, different schemes can be adopted according to different needs, and appropriate adjustments can be made.

6. Conclusion

This review paper presents SHE of GAAFET and its impact on the device. The formation mechanism and phenomenon of SHE in GAAFET is highlighted in a detailed discussion, compared with that in FinFET. This paper examines existing solutions for reducing the impact of SHE and provides comments on their advantages and limitations. It can be expected that as the device size further reduces, more severe degradation caused by SHE will become a vital problem for device lifetime and performance. In future researches, different working conditions can be key to addressing SHE, such as different transistor materials and gas pressures. Reducing the number of nanowires and reducing the thermal coupling effect are also promising research directions.

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