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Comparison and Performance Optimization of Two Absolute Circuit Designs Based on Multisim

Haoxiang Li[1,a,*]

[1]*Xiamen University,422 Siming South Road, Siming District, Xiamen City, Fujian Province, China*
a. 37720222204933@stu.xmu.edu.cn
**corresponding author*

Abstract: Digital circuits are crucial in today's technology, underpinning infrastructure such as computing, communicating, and intelligent devices. Its high efficiency, accuracy and programmable capability drive the development of information processing, data transmission and automation systems. The application of digital circuits has promoted innovation in artificial intelligence, the Internet of Things and other fields, providing strong support for the intelligence and interconnection of modern society. The absolute value circuit is discussed in this paper. The absolute value circuit is implemented for converting the negative value of the input signal to a positive value, ensuring that the output signal is always non-negative. Its significance is to handle application scenarios that require non-negative values, such as signal processing, audio amplification, and sensor output. Through the absolute value circuit, negative value can avoid the negative effect on the subsequent circuit, and improve the stability and accuracy of the system. This paper first introduces all the gates used in the circuit, points out the functions of each gate circuit, and then puts forward two absolute value circuit designs, explaining their working principles, differences and advantages and disadvantages. Then the minimum delay is analyzed by the critical path logic and the sizes of each logic gate is given. Then the supply voltage is optimized after selecting the design with the smallest delay to reduce energy consumption.

Keywords: Digital circuit, absolute value circuit, electronic engineering.

1. Introduction

Digital circuits have a profound significance in today's society, affecting almost every aspect of our lives. With the development of science and technology, digital circuits have become the core of modern electronic equipment, whether it is smart phones, computers, automobiles and medical technology [1], digital circuits play a key role in them.

Digital circuits promote the advancement of information technology. In the process of the popularization of computers and the Internet, digital circuits are the basis for realizing high-speed computing and data transmission [2,3]. The central processing unit, memory, and other key components of modern computers rely on complex digital circuit designs. These technological advances not only enhance computing power, but also support the development of cutting-edge fields such as artificial intelligence and big data analysis [4-6].

This paper discusses the absolute value circuit in digital circuit, which has strong application value. In some applications, negative voltages can cause damage to equipment. Absolute value circuits can

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avoid this and protect subsequent circuits from negative voltage. In audio processing and communication systems, signals often need to be kept positive for further analysis and processing [7]. The absolute value circuit ensures that the signal remains consistent during processing. In statistics and data analysis, absolute values are used to calculate bias and error. Absolute value circuits can be used for real-time signal processing, providing absolute deviation values that help adjust circuit accuracy [8,9].

This paper first introduces the gate circuit used in the circuit, then discusses the two absolute value circuit designs and the advantages of choosing this design, and then compares the minimum path delay of the two through critical path logic analysis, and selects the better one, that is, the one with the smaller critical path minimum delay, to optimize the supply voltage to reduce energy consumption.

The first chapter of the paper is the introduction, which first introduces the research background and significance of the paper. The second chapter is the main part, which gives the research content and research process. The last part is the conclusion, which summarizes the whole paper.

2. Introduction of gate circuits used in the circuit

2.1. Inverter

There is only one input and one output within an inverter, and its function is to invert the input signal. When the input is logic high level, the output is logic low level. When the input is logic low level, the output is logic high level. Table1 gives the truth table of the non-gates used.

Table 1: The truth table of the inverter

A	B
0	1
1	0

2.2. Transmission gate

A transmission gate is an analog switch that transmits an analog signal. The CMOS transmission gate consists, in parallel, of an N-channel and an P-channel enhanced MOSFET. The left side of the transmission gate is the input side, and the right side is the output side. The control signal input is on the upper side and the lower side of the gate Table2 gives the truth table of the transmission gate used.

Table 2: The truth table of the transmission gate

C	A	B
0	0	Hi-Z
0	0	Hi-Z
1	1	1
1	1	0

2.3. 2-input XOR gate

An XOR gate has one output and two inputs. The condition that the output is logically high level is that the input signals are different, that is, one is high level and the other is low level. If the two input signals are the same, the output is logically low. Table3 shows the truth table of the two input XOR gates used.

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Table 3: The truth table of the XOR gate(2-input)

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

2.4. 2-input NAND gate

A two-input NAND gate has two inputs and one output, which is logically low when all inputs are logically high, and logically high when the output is otherwise high.

Table4 shows the truth table of the two input NAND gates used.

Table 4: The truth table of the NAND gate(2-input)

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

3. Circuit design advantage

First, absolute value circuits in this article are built using CMOS. The CMOS circuit has a low energy consumption, so that it can be applied to some scenarios with more stringent energy requirements. Second, CMOS circuits can allow for higher integration density, so that more logic gates can be concentrated in the smallest space possible, improving space utilization efficiency.

Besides, ripple carry adders are implemented in the circuits. Common adders, in addition to the ripple carry adder, also include carry bypass adder, carry select adder. But the input for this experiment is a 4-bit binary number. When the number of input binary digits is 4 bits, the circuit delay can be minimized by using a ripple carry adder [10].

4. Circuit design

4.1. Function description

In this circuit, the input first passes through the adder part. If the 4-bit binary number is positive, that is, the highest bit is "0", this part can be ignored. If the input is negative, that is, the highest bit is "1", then you will first flip and add 1 to convert it to the corresponding positive number. The data then passes through the data selector section. If the 4-bit binary number is positive, that is, the highest bit is "0", then the NMOS input of transmission gate 1, 3, and 5 is low, and the PMOS output is high, which is high impedance state. 2, 4, and 6 transmission gates The NMOS input is high, and the PMOS output is low, indicating the on-state. At this time, the number will be transmitted through the transmission gate 2, 4, and 6 to reach the output end. If the input is negative, that is, the highest bit is "1", then the input at the NMOS end of transmission gate 1, 3, and 5 is high, and the output at the PMOS end is low, which is the on-state. 2, 4, and 6 transmission gates NMOS end input is low, PMOS end output is high, high impedance state, then the digital will be transmitted through 1,3,5 transmission gates to reach the output end.

Figure 1 and Figure 2 respectively show the circuit diagram of the circuit constructed by two methods.

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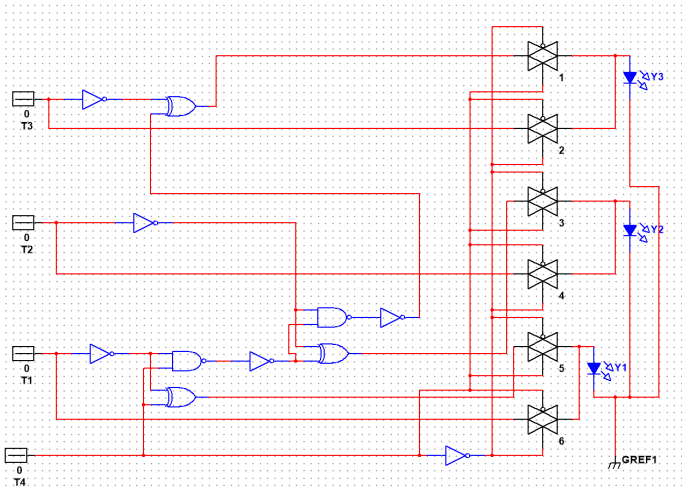

Figure 1: Absolute-value circuit topology using XOR and NAND gate

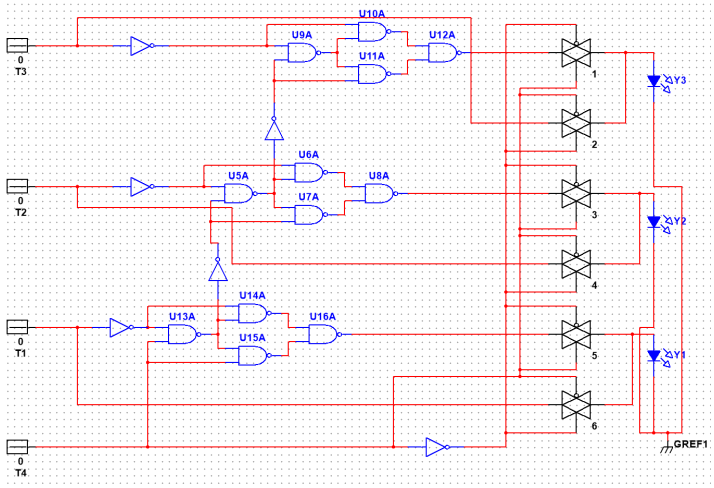

Figure 2: Absolute-value circuit topology using NAND gate

Table 5 gives the truth table of the absolute value circuit.

Table 5: The truth table of the 3- bit absolute-value circiut

T4	T3	T2	T1	Y3	Y2	Y1
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	1	0	0
0	1	0	1	1	0	1
0	1	1	0	1	1	0
0	1	1	1	1	1	1
1	0	0	1	1	1	1
1	0	1	0	1	1	0
1	0	1	1	1	0	1
1	1	0	0	1	0	0

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Table 5: (continued).

1	1	0	1	0	1	1
1	1	1	0	0	1	0
1	1	1	1	0	0	1

4.2. Design ideas

First of all, the use of the transmission gate to filter out the positive number first, can greatly reduce the delay when the input is positive, second, the half adder is generally composed of a logic gate to calculate the output bit and a logic gate to calculate the carry, but in the calculation to Y2, because it is the highest bit, so the half adder does not need to calculate the carry, at this time can eliminate a logic gate to calculate the carry. Finally, there are two design methods for the half adder, one is to build the half adder entirely using NAND gates, and the other is to build the half adder using XOR gates with NAND. A half-adder built using XOR gates and NAND gates can reduce the parasitic delay on the critical path compared to a half-adder built using only NAND gates, but the branching effort is correspondingly increased and the number of logic gates on the critical path is reduced, so both designs need to be further explored.

5. Circuit optimization

5.1. Critical Path Analysis

Firstly, the critical paths in the two circuits are mapped, which are given in Figure 3 and Figure 4 respectively.

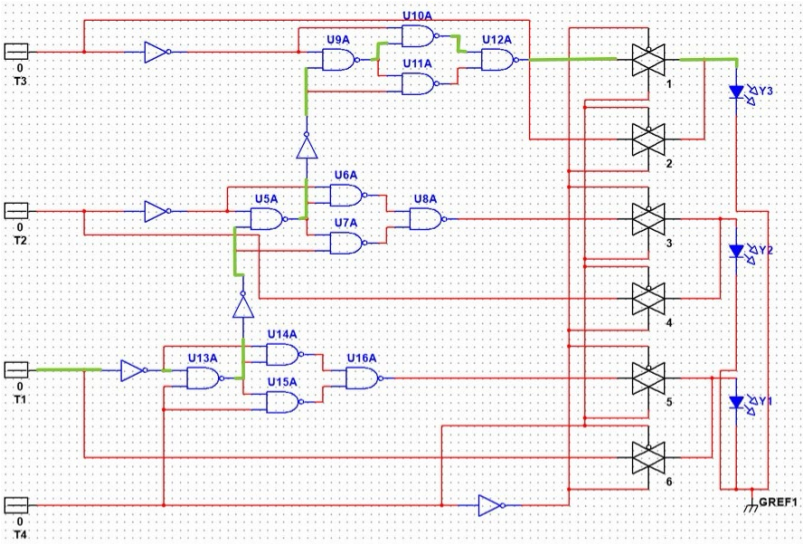

Figure 3: Critical path of the absolute-value circuit using NAND gate

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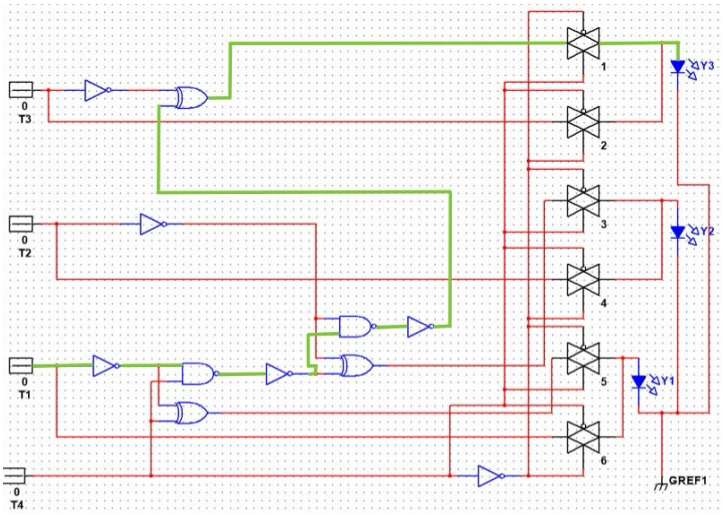

Figure 4: Critical path of the absolute-value circuit using XOR gate and NAND gate

In this experiment, the applied CMOS Wp = 650nm, Wn = 430nm, Lp = Ln = 100nm.

From the critical path, the circuit gate effort is calculated by formula (1). Where the total logical effort of the gate path is G, the total electrical effort is H and the total branching effort is B. g of different logic gates is given in Table 6.

Table 6: Logic effort(g) for different gates

Gate	g
inverter	1
NAND gate(2-input)	4/3
XOR gate(2-input)	4

$$F = GBH \tag{1}$$

Next, determine the number of gates N on the path, and then calculate the circuit minimum gate effort by formula (2)

$$f^* = F^{\frac{1}{N}} \tag{2}$$

Next, the minimum delay D of the circuit is calculated by formula (3), and p is the parasitic delay, which can be calculated by formula (4). The p of different logic gates is given in Table 7.

$$D = N * f^* + \sum p \tag{3}$$

$$p = \frac{C_{input,gate}}{C_{input,inverter}} \tag{4}$$

Table 7: Parasitic delay(p) for different gates

Gate	p
inverter	1
NAND gate(2-input)	2
XOR gate(2-input)	4

Next, from output to input, the dimensions of each logic gate are calculated by formula (5).

$$C_{in} = g\frac{C_{out}}{f^*} \tag{5}$$

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Taking the total electrical effort as 16 first, after this calculation process, it can be obtained that the minimum delay of the absolute value circuit using only NAND gate is 35.92, while the minimum delay of the absolute value circuit using XOR and NAND gate is about 31.7, so it is better to use XOR gate and NAND gate when building this absolute value circuit.

Next, the dimensions of each logic gate are calculated by formula (5), and the Figure 5 presents the calculation results.

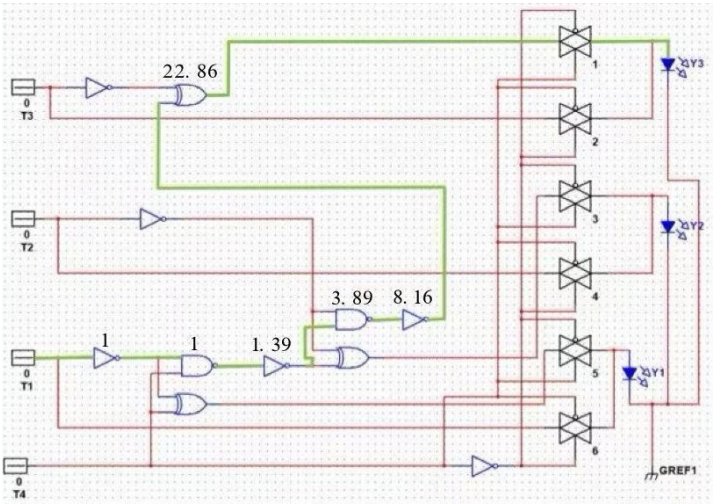

Figure 5: Absolute value circuit logic gate size

5.2. V_{DD} optimization

V_{DD} also affects the delay and energy consumption of the circuit. When the line. In this design, the relationship between V_{DD} and the minimum delay of the line can be expressed by formula 6.

$$D \propto \frac{V_{DD}}{(V_{DD}-V_{TH})^2} \tag{6}$$

The CMOS threshold voltage used in the line is 0.2V. Due to the need to reduce energy consumption, the latency was increased to 1.5 times to achieve this goal.

$$\frac{D}{1.5D} \propto \frac{\frac{1}{(1-0.2)^2}}{\frac{V_{DD}}{(V_{DD}-0.2)^2}} \tag{7}$$

According to formula (7), the best is 0.776V or 0.05V (omitted because it is less than the threshold voltage). Equation (8) is used to calculate energy consumption.

$$E = C_{path} * V_{DD}^2 \tag{8}$$

At this time, the circuit energy consumption is reduced by 80% compared with the energy consumption corresponding to the minimum energy consumption, although the delay is increased by 1.5 times, but this is acceptable.

6. Conclusion

In this paper, the design of two absolute circuits with the smallest delay is successfully selected and the energy consumption of which is reduced by 80% under the condition of acceptable delay.

The relationship between V_{DD} and line minimum delay is approximate and does not necessarily apply in other circuits.

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Absolute value circuits are expected to achieve innovative applications in many fields in the future. As technology advances, it can achieve more efficient performance on smaller chip sizes, supporting more complex signal processing tasks. In addition, combined with artificial intelligence and the Internet of Things, absolute value circuits will play a more important role in smart devices, automated systems and precision measurement, improving processing speed and accuracy.

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