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Research on Optimization of High-Speed Low-Power Digital Circuits

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Abstract: As electronic devices become increasingly portable and mobile, how to extend the battery life of these devices while ensuring performance has become a great challenge for engineers. This paper studies the design of the basic circuit and how to balance the relationship between high speed and low power consumption, proposing an effective optimization method. Specifically, the method includes the optimization of the transistor size of the critical path and the methods for the optimization of the supply voltage. This kind of method is of practical significance for the optimization of basic circuits and enlightenment for the optimization of large-scale integrated circuits

Keywords: high speed, low power design, power optimization, absolute value detector.

1. Introduction

Nowadays, with the rapid development of digital integrated circuit (DIC) technology and the increasing integration of mobile devices, the demand for high-speed, low-power processor designs has grown significantly [1]. This is especially critical when we come to mobile phones or smart watches, where battery capacity is limited, making it essential to reduce energy consumption without influencing or even improve performance.

To make this vision a reality, significant efforts have been made and substantial progress has been achieved in various areas, such as minimizing transistor size [2], redesigning transistor structures with new materials[3], and applying software optimization techniques[4].

This paper will focus on the design and optimization of basic circuits, specifically discussing the high-speed, low-power optimization of a typical circuit in CMOS structures—the absolute value comparator.

2. Research on the high-speed and low-power absolute value detector based on CMOS structure circuits

This section explores design strategies for circuit structures, using a 4-bit absolute value comparator as a detailed example. It also provides analysis and discussion on the optimization of delay and power consumption in the circuit.

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2.1. Circuit structure design research

The function of the absolute value detector is to compare the absolute value of the input with the threshold, which is pre-inputted, and output the comparison result (if the input is greater than the threshold, output 1, otherwise output 0). To achieve this function, the entire circuit can be roughly divided into two basic function building blocks: an absolute value adder and a comparator. The logic structure of the overall procedure is roughly shown in Figure 1.

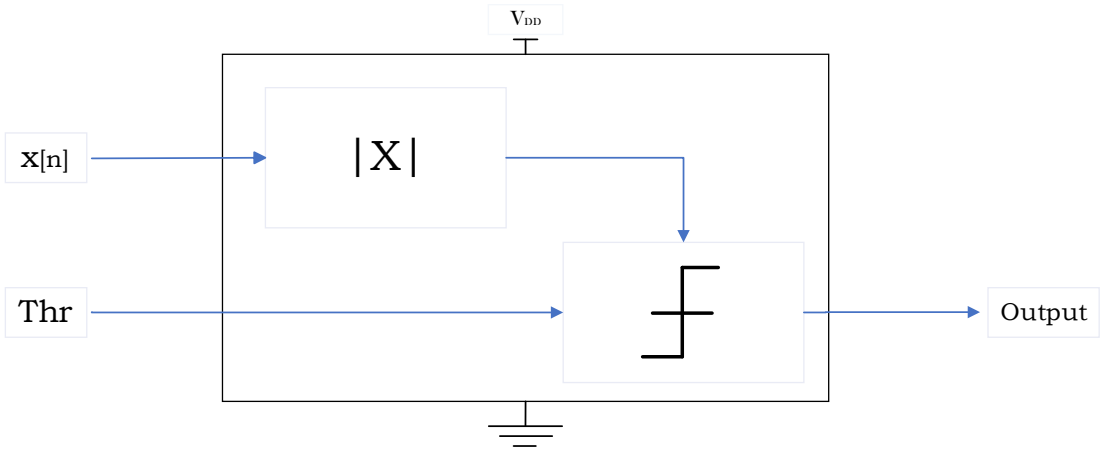

Figure 1: Overall Procedure for Absolute Value Detector

First, for the absolute value adder, since the most significant bit (MSB) in binary code represents the sign, the actual implementation of the function of taking the absolute value should be expanded as: first judge the sign bit, then if the sign bit is 1 (indicating a negative number), the two's complement is taken; if the sign bit is 0 (indicating a positive number), no operation is performed. Subsequently, for the comparator section, the processed data will be used as input to the comparator and compared to the pre-inputted threshold.

In the design of the entire circuit, the strategy focusing on minimizing the critical path and simplifying the circuit as much as possible should be adopted. Additionally, advanced CMOS technologies such as FD-S0I or FinFET [5] can be applied to further improve the performance of the circuit.

Follow the above strategy, this paper takes a 4-bit absolute value detector as an example to propose a reference circuit, as shown in Figure 2:

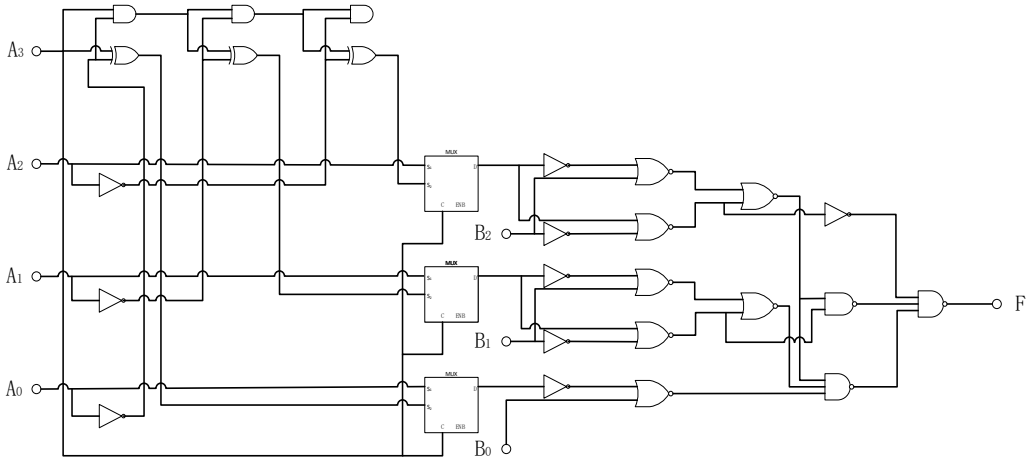

Figure 2: Reference Circuit for 4-bit Absolute Value Detector

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Since positive numbers and negative numbers are different only in the most significant bit (MSB), this paper proposes using mux [6] in the circuit, with the sign bit A3 is used as the control bit of mux to control the output of mux. When the sign bit is 0, MUX selects the output of the original signal; When the sign bit is 1, the MUX selects to output a signal that has been negated and added to one (two's complement). Meanwhile, since the sign bit does not participate in the subsequent comparison, the output of the absolute value adder is only three digits, and the comparator only needs to realize the function of three digits.

Besides the comparator implemented with logic gates as proposed in Figure 2 above, a binary digital logic comparator based on half adders [7] can also be used. The principle of this comparator is to compare the inputs bit-by-bit from the most significant bit. If the inputs A_i and B_i are equal, the Sum output 1. Then the next bit is compared. The sum of each bit is then ANDed together. If the output is 1, means A and B are equal. If the inputs of A_i and B_i are not equal, then Carry outputs 1, and the Carry signal is ANDed with A. If the result is zero, indicating that it is $A < B$, otherwise, $A > B$. Only 3 half-adder circuits are required to compare 3-bit binary numbers.

The circuit proposed in this paper has a clear logical function, characterized by a simple critical path, low delay, and low power consumption. More importantly, the circuit is scalable, it is easy to extend for a higher-bit absolute value detector circuits based on this structure.

2.2. Research on circuit delay optimization

The overall delay of the circuit is mainly determined by the delay of the critical path, which has been basically determined once after the circuit structure is determined. Any optimization of the circuit's delay must be built on this foundation. The main direction for optimization is the redesign of transistor sizes (sizing) to reduce overall delay. Additionally, when selecting transistors, important parameters such as mobility, gate voltage, and current drive capability should be considered [8]. Generally, transistors with high mobility and low threshold voltage are better suited to meet the requirements of high speed and low power consumption. However, better performance always means the much more expensive price.

When analysing and calculating the delay of the critical path, the following formulas and algorithms are typically used for derivation [9].

$$f^* = \sqrt[N]{Patheffort} \tag{1}$$

$$f^N = \Pi g \cdot h = Patheffort \tag{2}$$

$$C_{in} = g\frac{C_{out}}{f^*} \tag{3}$$

Therefore, when sizing the critical path, the process typically comes as step-by-step derivation and optimization from the back to the front. The detailed calculations and optimization processes will not be discussed in depth in this paper.

2.3. Research on circuit power consumption optimization

The overall power consumption of the circuit can be divided into dynamic power, static power, and short-circuit power. The part that can be primarily optimized is the dynamic power [10]. According to the formula for calculating dynamic power:

$$P = \alpha C_L V_{dd}^2 \tag{4}$$

The primary direction for optimizing dynamic power is to reduce the supply voltage. Additionally, optimizing the load capacitance (C_L) during the sizing process can also be considered.

For a given circuit, optimizing the supply voltage V_{dd} will inevitably increase the delay. The challenge lies in finding the optimal supply voltage within the desired delay range. For example, if

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the lowest delay is identified at a preset supply voltage, the goal is to find the most suitable supply voltage that allows the delay to remain within 1.5 times the minimum delay. This involves exploring how much the supply voltage can be reduced while still meeting the performance requirement of 1.5 times the minimum delay.

Because:

$$d \sim \frac{V_{dd}}{(V_{dd} - V_T)^2} \tag{5}$$

Where d is the delay of one gate. Assume that $V_T = 0.2V$, the expected delay factor DF for the delay D of the circuit satisfies the following relationship:

$$DF = \frac{0.8^2}{(V_{dd}^* - 0.2)^2} V_{dd}^* \tag{6}$$

Regarding V_{dd}^* as the independent variable and DF as a function of V_{dd}^*, it can be observed that as V_{dd}^* decreases, DF increases. Therefore, for a given range of $1 \leq DF \leq 1.5$,when $DF = 1.5$, it can be determined that$V_{dd}^{opt} = 0.776 V_{dd}$. This means that when the supply voltage is set to 0.776 times the preset voltage, the minimum power consumption can be achieved while keeping the delay within the required range.

2.4. The high speed and low power consumption

Based on the analyses in sections 2.2 and 2.3, there is a fundamental approach in optimizing the circuit's delay and power consumption. However, it should be noted that the optimization directions in 2.2 and 2.3 have conflicts with each other. For instance, in 2.2, increasing the supply voltage can reduce the circuit's delay, but this will also increase the power consumption as discussed in 2.3. The same applies to sizing: while increasing the transistor width can reduce delay, it also leads to higher power consumption.

Also, it is worthy to know that optimizing for low power while ensuring a specific delay is quite challenging, as it requires individual optimization of each transistor's size. This challenge becomes exponentially more difficult in larger circuits. However, reducing power consumption while maintaining a fixed delay is generally easier. Therefore, in practice, the common strategy is to first optimize the delay and then adjust the supply voltage according to the required delay factor.

Lastly, it should be emphasized that the optimization goal should always be finding a balance between maximum speed and minimum power consumption. The target balance point must be considered in conjunction with practical engineering requirements.

3. Conclusion

This paper discusses the design and optimization strategies for basic circuits in digital integrated circuits, using an example of CMOS-based absolute value detector and provides a detailed discussion of both delay and power consumption, presenting specific optimization methods: reducing delay can be achieved through step-by-step sizing derivation and optimization of the critical path from back to front; reducing power consumption can be accomplished by lowering the supply voltage. The paper also explores methods for determining the minimum supply voltage based on the target delay range. Ultimately, the analysis leads to the perspective that optimizing for high speed and low power consumption is to find a balance between the two, while emphasizing the importance of considering practical engineering constraints in the process also worthy.

The discussions in this paper are intended to help relevant professionals better understand the concept of high speed and low power consumption, and to provide insights into the optimization and design of basic circuits. However, it is important to note that the research is limited to specific

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examples, and its applicability to more complex circuit designs may be limited. Future studies are encouraged to expand research on the design and optimization of more complex circuits.

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