Proceedings of the 5th International Conference on Materials Chemistry and Environmental Engineering
DOI: 10.54254/2755-2721/123/2025.19591

Analysis and Design of High Speed and Low Power Digital Integrated Circuits

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Abstract: With the continuous improvement of performance and energy efficiency requirements for electronic devices, high-speed and low-power technology has become a research hot spot. This paper aims to explore the balance between high-speed signal transmission and low power consumption, and introduces various optimization strategies, including circuit design, material selection, and architecture improvement. By adopting new semiconductor materials and advanced power management technology, this article examines the mechanics underlying power consumption and delay generation and presents strategies for optimizing circuit architecture to create digital integrated circuits that are both fast and low-power, optimizing materials, and variable VDD/VTH control, etc. The results show that the proposed method has good feasibility and practical application value in achieving the goal. Finally, this article provides an outlook on the future development trends of high-speed and low-power technologies, providing important references for research in related fields.

Keywords: high-speed,low-power, digital integrated circuits.

1. Introduction

As technology advances, integrated circuit design continues to see improvements in chip integration and speed, yet power consumption per unit area has not increased. Low power design is very important for extending battery life, optimizing battery performance, and achieving miniaturization of battery powered equipment. At the same time, with the development of the times, people's requirements for the operating speed of various electronic products are increasing. Since power consumption is approximately proportional to the square of the power supply voltage, lowering the power supply voltage is the most effective method of achieving low power performance in digital CMOS circuits [1].Formulas (1) and (2) illustrate how they relate to the power supply voltage V_{dd}:

$$P \approx C_l V_{dd} 2 f_{OP} \tag{1}$$

$$t_{pd} \propto C_l V_{dd} / I_{ds} \propto C_l V_{dd} [A(V_{dd} - V_{th})^2]^{-1} \tag{2}$$

Currently, most literature only focuses on the analysis and research of low power consumption, while there is relatively little research on achieving high-speed and low power consumption. Optimizing power consumption while improving the speed of integrated circuits is currently a problem that every IC design company needs to consider. Given that power consumption and circuit delay are positively correlated with voltage and power supply, the implementation of low power

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DOI: 10.54254/2755-2721/123/2025.19591

consumption will come at the cost of sacrificing some speed. For example, in computers, a large amount of heat is inevitably generated while achieving high-speed operation. To solve the above problems, this article first analyzes the composition of power consumption, improves the circuit structure by using FinFET materials, reduces node capacitance, and regulates voltage to achieve low power consumption. Then, the mechanism of delay generation is analyzed to find possible design methods that can simultaneously achieve high power consumption and improve the method of implementing low power circuits.

The main structure of this article is as follows: Chapter 1 is the introduction, which first introduces the research background and significance of the paper. Chapter 2 is about the composition of power consumption, providing circuit parameters related to power consumption. Chapter 3 is about the design method of low-power circuits. Chapter 4 jointly considers power consumption and delay to provide a design method for high-speed low-power circuits. Finally, the conclusion section summarizes the entire paper.

2. The generation of the power consumption

The total power consumption of digital integrated circuits can be divided into two groups: static power consumption and dynamic power consumption. The following Equation (3) illustrates their relationship.

$$P = P_d + P_s \tag{3}$$

The dynamic and static power consumptions are denoted by Pd and Pst, respectively.

2.1. Static power consumption

Static power consumption is generated by static current. Due to previous technological limitations, the static power consumption caused by static current can be ignored. However, with the development of low-voltage deep sub micron and ultra deep sub micron technologies, designers will increase static current. The disadvantage is that static power consumption increases, but it can achieve fast unit circuits[2]. From the formula it can be concluded that the magnitude of static power consumption is mainly related to V_{dd} and static current. Their relationship can be shown by Equation (4) below.

$$P_{st} = V_{dd} \times I_{leak} \tag{4}$$

2.2. Dynamic power consumption

Switch power consumption and short power consumption are the two categories into which dynamic power consumption may be divided. The following Equation (3) illustrates their relationship.

$$P_d = P_{sw} + P_{sh} \tag{5}$$

2.2.1. Power consumption of the switch

CMOS transistor power consumption brought on by modifications to circuit logic, including flip power consumption, refers to the power consumption of load capacitors during charging and discharging, as well as the phenomenon of competitive risk. This phenomenon is similar to the principle of flip power consumption, but the phenomenon of race and hazard is caused by useless jumps in the circuit, which are caused by the normal operation of flip power circuits.It can be represented by Equation (6):

$$P_{sw} = \alpha f C_L V_{dd} 2 \tag{6}$$

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CL is the equivalent load capacitance of CMOS transistor, α is the probability of circuit state flipping per unit time, f is the operating frequency of the circuit, VDD is the voltage power supply, also known as logic swing[3].

2.2.2. Short power consumption

There are two main factors that affect short-circuit power consumption:working voltage V and short-circuit current I. When the P-type and N-type transistors are both on simultaneously during the MOS transistor circuit's switching process, a current known as the short-circuit current is produced.Equation (7) below illustrates their relationship [4].

$$P_{sh} = V_{dd} \times I_{sh} \tag{7}$$

In summary, we can determine that the power consumption of digital integrated circuits is caused by three main sources: static power consumption, switch power consumption, and short power consumption. The planar diagram of CMOS power consumption composition is shown in Figure 1, and the relationship between static power consumption, flip power consumption, and short-circuit power consumption is shown in Equation (8) below.

$$P = P_{st} + P_{sw} + P_{sh} \tag{8}$$

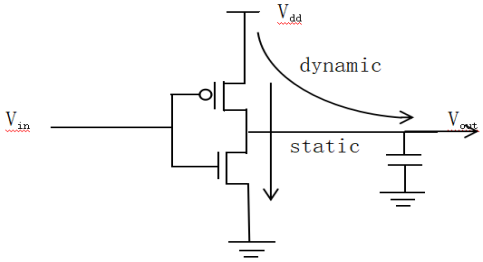

Figure 1: Power consumption component of CMOS.

3. Low power design of digital integrated circuits

Dynamic power consumption is the primary force behind CMOS power consumption. Power consumption can be successfully decreased by lowering the power supply voltage, node capacitance, and switch activity, as the preceding paragraph makes clear.

When improving V_{dd}, the delay of the circuit will increase significantly when it approaches the threshold voltage (V_{th}). In general, the VDD is not less than 2-3 times the V_{th}, and a lower V_{th} is used to maintain circuit performance. However, V_{th} cannot be too small, otherwise a certain noise threshold Noise Margin cannot be maintained, and the power consumption caused by leakage current will also greatly increase [5].

Circuit capacitors are divided into three parts: gate capacitors, diffusion capacitors, and interconnect capacitors. To comprehensively consider and design the performance, power consumption, and area in numbers, the goal of minimizing area and power consumption is generally consistent [5]. Therefore, in low-power integrated circuit design, optimization can be carried out at the cost of chip area and performance when necessary.

3.1. The adoption of FinFET technology

Using FinFET instead of traditional MOSFET can effectively reduce short channel effect and leakage current, thereby reducing power consumption. FinFET is a field-effect transistor, which has two characteristics compared to traditional planar devices. Firstly, it solves the leakage problem while reducing the critical size. Solving the leakage problem can significantly improve chip performance

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and reduce power consumption; Secondly, the three-dimensional structure transforms the transistor structure from horizontal to vertical, achieving upward development and greatly improving integration[6]. The structure of FinFET is shown in the following figure 2:

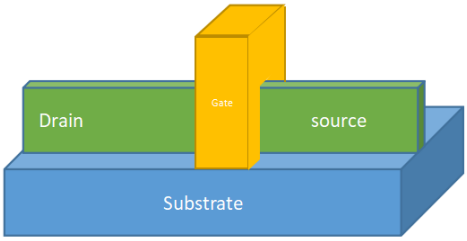

Figure 2: 3D structure of FinFET.

One of the primary challenges in scaling down traditional CMOS technology is that, despite the reduction in IC size achieved through transistor scaling, short channel effects emerge when scaling exceeds the nanometer level. These effects result in increased leakage power, thereby augmenting overall power consumption. To mitigate the short channel effects and attain low power consumption, FinFET technology was introduced. FinFETs feature a gate surrounded by a structure known as a "fin". Compared to planar devices, FinFETs offer enhanced electrostatic control over charge carriers and greater current drive per unit area, thanks to the fin height and the gate's surrounding structure around the channel. This design enables smaller transistors to operate more efficiently, while concurrently reducing power consumption and latency. In the design and simulation of FinFET-based digital circuits, power consumption and delay stand as two pivotal parameters in integrated circuit design. When compared to traditional 45nm CMOS technology, FinFETs utilizing 22nm technology exhibit a notable reduction in power consumption. Specifically, circuits employing 22nm FinFET technology demonstrate superior performance in terms of power dissipation and delay, with significant improvements observed particularly in power dissipation. Consequently, the application of FinFETs provides research direction for further advancing low-power, high-performance integrated circuit design.[7].

3.2. Regulation and structural design of power supply voltage

Power consumption can be considerably decreased by lowering the operation frequency and power supply voltage. Equation (6) indicates a positive correlation between power and the power supply voltage squared. Consequently, one of the most efficient ways to lower power usage is to lower the power supply voltage.

This can be achieved through the design of a multi-power supply and multi-voltage structure. By implementing the power-off mode of the entire circuit, the dynamic and static power consumption of each independent circuit module can be controlled to be within the lowest standard range, resulting in the minimum total power consumption [8]. Dynamic Voltage Scaling (DVS) is a method of reducing power consumption by dynamically adjusting voltage and frequency. Super Dynamic Voltage Regulation (Super DVS) has been improved on the basis of traditional DVS to further reduce power consumption and improve system efficiency. According to current research, Super Dynamic Voltage Regulation technology can drastically lower SoC chip power usage. The algorithm and hardware implementation scheme have high efficiency and reliability, and the technology has good application prospects and is suitable for various low-power SoC designs [9] (Figure 3).

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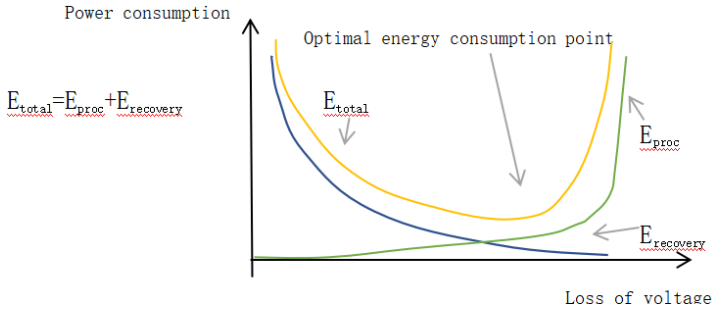

Figure 3: The relationship between operating voltage and system power consumption.

However, achieving low power consumption through voltage control still has certain limitations. Due to the fact that the turn-on voltage is still set high at 0.7V to 1.0V in most processes, when the operating voltage is reduced to 5V, it can achieve low power by reducing the leakage current of the secondary turn-on voltage, while also obtaining a large noise margin. However, when the operating voltage is less than 3.3V, this high turn-on voltage is not conducive to reducing the power supply voltage and power consumption.

3.3. Optimizing Circuit Architecture

The use of advanced circuit architectures such as clock gating technology and null convention logic (NCL) can significantly reduce power consumption. Clock gating technology can reduce dynamic power consumption by stopping the propagation of clock signals when not needed. The commonly used Clock Gating technology manages the clock network of each module at the chip level. When a sub-module in the chip enters an idle state, the corresponding clock branch will be turned off. This can be achieved by either shutting down the sub-module or eliminating redundant level flips in the clock network, thereby reducing power consumption. However, traditional clock gating still has limitations. When applied in large-scale circuits, there are a large number of registers in the circuit whose states do not change most of the time. The clocks of these registers undergo level flips over a large amount of time, which can generate a lot of power consumption. There are now studies to determine whether it is necessary to gate the clocks of the registers in order to further reduce power consumption [10]. NCL is a clock free circuit design technology that has gained attention in ultra-low power circuit design due to its flexibility and ease of use. NCL eliminates clock signals and avoids clock skew problems in traditional synchronous circuits. It adopts a delay independent design method, which enables the circuit to have stronger adaptability to data and environmental changes. This design method has significant advantages in both power consumption and area, making it particularly suitable for power sensitive application scenarios.

4. High-speed digital integrated circuit implementation

With the increasing demand for high-speed modern applications, various technologies and methods are constantly being developed and improved to enhance the speed of digital integrated circuits. The speed of digital integrated circuits is related to the resistance, length, number of logic gate transistors, and power supply voltage of the circuit, and is positively correlated with the voltage.

4.1. Optimizing circuit logic

Optimizing circuit logic can be divided into timing optimization methods and combinational optimization. Without altering the combinational logic relationship between registers, the combinational logic optimization method makes the input terminal of the register the circuit's primary

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output and the output terminal of the register the circuit's primary input. By locally adjusting the logic structure while ensuring the combinational logic function, the timing requirements can be achieved [11]. The optimization of combinational logic can be considered from the following two optimization perspectives. One is the traditional timing optimization problem. After performing static timing analysis (STA), under the guidance of STA, the logic or physical layout of the gates in the circuit is adjusted to optimize the timing. Then, in order to meet the timing requirements and minimize the delay in signal transmission, buffers are placed on the critical path. Finally, an optimized clock allocation network is created to reduce clock skew and mismatch Consider the timing performance of circuits under different operating modes and manufacturing process deviations to ensure that timing requirements can be met under various conditions. The second is statistical timing optimization, which aims to optimize the timing performance of circuits and increase circuit yield in the presence of process changes and other random factors. This can be achieved through a series of methods such as sensitivity analysis and gate level adjustment, statistical static timing analysis, and yield gradient optimization [12].

4.2. Material selection and voltage control

Choosing different materials and design strategies can significantly improve the speed of digital integrated circuits. Digital integrated circuits' speed, power usage, and voltage are all positively connected, but as the voltage rises, so does the power consumption. As a result, the voltage should adopt a suitable intermediate value when developing integrated circuits that are both high-speed and low-power. High-speed and low-power digital circuit technology has also improved speed performance while controlling power consumption by using MOSFETs with a low threshold voltage at a power supply voltage of 1V. Compared with traditional low threshold voltage CMOS circuits, multithreshold-voltage CMOS circuits achieve a better balance between energy consumption and performance. High-speed digital circuit design under a 1-V power supply is possible using multithreshold-voltage CMOS technology, which also strikes a solid balance between high performance and low power consumption [1].

5. Conclusion

In summary, the primary methods for creating integrated circuits with high speed and low power include the utilization of FinFET materials, clock gate technology for timing logic optimization, and MOSFETs with low threshold voltage for voltage control and regulation. However, although this article provides some solutions for the design of low voltage and low power digital integrated circuits, there are still many unresolved issues, such as the specific impact of FinFET materials on digital integration speed, the feasibility of optimizing timing logic while using clock gate technology, and currently only discussing the use of new materials to achieve high speed at the lowest possible voltage, achieving a balanced voltage between power consumption and speed. The impact of selected voltage on other functions of the circuit is still under discussion. At the same time, as the integration level of chips continues to increase, the size of materials and the difficulty of processes still need to be improved. It is still necessary to conduct in-depth research on how to ensure that digital integrated circuits maintain circuit performance and speed within the specified voltage, reduce voltage and power signal, and further reduce leakage current in design processes to achieve power consumption reduction.

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References

[1] S. Mutoh, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu and J. Yamada, "1-V power supply high-speed digital circuit technology with multithreshold-voltage CMOS," in IEEE Journal of Solid-State Circuits, vol. 30, no. 8, pp. 847-854, Aug. 1995.

[2] Jun Li. Low power analysis in digital integrated circuit design [J]. Journal of Zhaoqing University,2009,30(05):51-53.

[3] Changlin Wang, Yong Zhang, Dongsheng Li, Power consumption analysis and optimization methods for CMOS integrated circuits [J] Ship Electronic Engineering ,2006,26(3):123-125,166.

[4] Weijun Hu. Review on low power design of digital integrated circuits[J]. Journal of Physics Conference Series, 2024, 2798(1): 012047.

[5] Tao Zhong, Haocai Wang, Power Optimization and Low Power Design Techniques for CMOS Integrated Circuits [J]. Microelectronics,2000,(02):106-112.

[6] Qide Yao, Key Technology of SiGe High Mobility Channel Passivation and Its Application in FinFET Devices[D]. North China University of Technology, 2022.

[7] S. Greeshma Sai, N. Alivelu Manga, and P. Chandra Sekhar, "Design and Simulation of FinFET based digital circuits for low power applications," in 2020 IEEE International Students' Conference on Electrical, Electronics and Computer Science (SCEECS), Feb. 2020.

[8] Jingguo Chen, Gang Tian. Low power analysis in digital integrated circuit design [J]. Electronic components and information technology, 2023,7(06):144-147.

[9] Chen Shen, Research on Key Technologies for Super Dynamic Voltage Regulation of Low Power SoC Chips [D] Jiangsu: Southeast University, 2011.

[10] Bangping Leng, Jianming Zhao Discussion on Low Power Design Technology of Digital IC Based on Gated Clock [C]// Proceedings of the 15th National Conference on Semiconductor Integrated Circuits and Silicon Materials 2007:145-148.

[11] Dan Shen Logic optimization of high-speed digital integrated circuits [D] Shanghai: Shanghai Jiao Tong University,2001.

[12] H. . -F. Jyu and S. Malik, "Statistical timing optimization of combinational logic circuits," Proceedings of 1993 IEEE International Conference on Computer Design ICCD'93, Cambridge, MA, USA, 1993, pp. 77-80.